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Numerical Simulation of the Comparative Electrical Performance of the Permeable Base Transistor, Opposed Gate-Source Transistor and Heterostructure Launched Ballistic Field Effect Transistor

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19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Devices operate under large signal conditions. Thus large signal simulations are required. This is illustrated for the permeable base transistor, the heterostructure bipolar transistor and the opposed source-gate transistor. There were a number of ground-breaking results during the course of this study. The most significant is that a simulation was developed that coupled the large signal two dimensional device behavior to the large signal properties of an external circuit. The study was applied most extensively to the permeable base transistor, where it was determined that if fabrication properties could be addressed successfully, the permeable base transistor could be a significant device in terms of output power and frequency. These results are summarized in the discussion of the permeable base transistor. Studies on the heterostructure bipolar transistor confirm that the long recombination times serve to yield superior performance for the indium based HBTs. Finally, the discussion of the OGST points to its promise as a high frequency switching devices. These studies were performed under Contract N00014-86-C-0567. This document summarizes the work under this contract.

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TRANSPORT CALCULATIONS AND EHF DEVICES

I. INTRODUCTION

Output power, efficiency and gain have always been key figures of merit for assessing the electrical characteristics of microwave and millimeterwave tube or solid state amplifiers; and device and circuit engineers exert considerable effort to optimize these quantities. Optimization has traditionally centered around such issues as the bias dependence of transconductance, circuit harmonic termination, etc. Typical studies of optimization procedures generally involve the coupling of circuits to **circuit representations of devices,** in, e.g., class A, B or C operation. Each of these studies is made extremely complex when dealing with solid state devices because of the inherent scattering mechanisms, the associated delay times, and the highly nonuniform space charge distribution within each device structure.

The issue that has plagued solid state device engineers and physicists is that of determining the best means of incorporating the space charge effects and scattering in the device models. The typical approach has been to examine the small signal properties of the device, derive empirical formulae with parameters that can be adjusted to fit measurement and then extrapolate to large signal behavior. From the point of view of a device engineer this is highly satisfactory, in that the models are often amenable to simple circuit representations of devices. Since these formule have been sufficiently reliable at frequencies near 1 GHz there has been a tendency to use them at much higher frequencies, **where they inevitably breakdown.** Thus at high frequencies other means must be imposed for examining device behavior. What are these means?

Devices operate under large signal conditions. Thus large signal simulations are required. This is illustrated for the permeable base transistor, the heterostructure bipolar transistor and the opposed source-gate transistor. There were a number of ground-breaking results during the course of this study. The most significant is that a simulation was developed that coupled the large signal two dimensional device behavior to the large signal properties of an external circuit. The study was applied most extensively to the permeable base transistor, where it was determined that if fabrication properties could be addressed successfully, the permeable base transistor could be a significant device in terms of output power and frequency. These results are summarized in the discussion of the permeable base transistor. Studies on the heterostructure bipolar transistor confirm that the long recombination times serve to yield superior performance for the indium based HBTs. Finally, the discussion of the OGST points to its promise as a high frequency switching devices. These studies were performed under Contract N00014-86-C-0567. This document summarizes the work under this contract.

II. DEFINITIONS

Class A, B and C Operation: Typical device operation is classified as either class A, B, or C. Under class A operation the gate bias and alternating gate voltages are such that the magnitude of the gate voltage never exceeds the pinchoff voltage. Class A operation has often been referred to as linear, although it need not be if the gate voltage undergoes

sufficiently large swings. Under class B operation the dc gate bias is close to pinchoff with the alternating voltages centered about pinchoff, the resulting drain current is highly nonlinear with values of gate bias in excess of pinchoff resulting in very small values of drain current. Under class C operation the dc gate voltage is substantially in excess of the pinchoff voltage.

SMALL SIGNAL CONCEPTS: POWER, GAIN, EFFICIENCY

The small signal admittance of a three terminal device is:

(1) $$\delta I_g = y_{11}\delta V_g + y_{12}\delta V_d$$

$$\delta I_d = y_{21}\delta V_g + y_{22}\delta V_d$$

where δI_g, δI_d, δV_g and δV_d represent small signal changes in the gate and drain potentials. If in the drain loop the load admittance is y_ℓ,

(2) $$\delta I_d + y_\ell \delta V_d = 0$$

and:

(3) $$\delta I_g = [y_{11} - y_{12}y_{22}/(y_{22} + y_\ell)]\delta V_g$$

$$= y_g \delta V_g$$

The input power is

(4) $$P_{in} = y_g \delta V_g^2$$

The power delivered to the load is

(5) $$P_{out} = -y_\ell \delta V_d^2$$

$$= -y_\ell [y_{21}/(y_{22} + y_\ell)]^2 \delta V_g^2$$

and the power amplification is obtained from the real part of:

(6) $$PA = P_{out}/P_{in} = y_\ell [y_{21}/(y_{22} + y_\ell)]^2 / y_g$$

Thus in the simplest case the power amplification may be obtained from the small signal admittance parameters of the transistor and the drain load. The power gain is:

(7) $$G = 10\log_{10}|PA|$$

There are several other quantities of interest. If $-y_\ell \delta V_d^2$ is the ac power delivered to the load, and P_{dc} is the dc power delivered to the device by the drain power supply, the drain efficiency is defined as:

(6) $$\eta_d = P_{in}/P_{dc}$$

The power added efficiency is defined as:

(7) $$\eta_{add} = \eta_d[1-1/G]$$

While it is known that the above admittance coefficients are bias dependent, operation of a device based upon these coefficients is often referred to as linear amplification, even though the output will sometimes depend upon the input level.

The above terms are those that are most familiar to the solid state device community. In the course of the study we had the opportunity to examine, in detail, the usefulness of these concepts for large signal operation, and have found them to be useful only as limiting situations of highly nonlinear phenomena. In the discussion that follows the large signal behavior of solid state devices was examined by implementing time dependent large signal device algorithms. In a typical large signal power calculation, as shown in figure 1, the gate was driven by an ac voltage and the drain contact was typically connected to a dc source through a load that was either resistive or contained reactive components. The ac input power to the device was obtained from the equation:

(8) $$P_{in} = (1/T)\oint [I_g(t)-<I_g>][V_g(t)-<V_g>]dt$$

where the brackets '< , >' denote dc averages, and T denotes the period of the oscillation. In the study the harmonic content of the oscillation was obtained by Fourier analysis. The

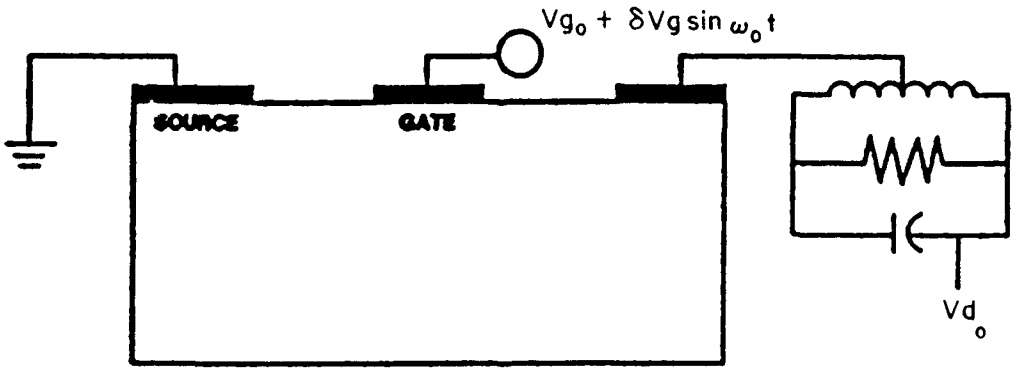


Figure 1. Schematic of the large signal calculation. A three terminal device is driven by a dc plus ac bias at the gate contact. Power is delivered to the load. The load is represented as a reactive circuit, the simplest one being that shown above.

power delivered to the load was calculated from:

(9) $$P_{out} = (1/T)\oint [I_d(t) - \langle I_d \rangle][V_{do} - V_d(t) - \langle V_d \rangle]dt$$

With the power amplification and gain given by equations (4) and (5).

When detailed comparison with small signal parameters was necessary, these were obtained numerically. For a given value of gate and drain bias, the potential at the gate (drain) was held fixed while the potential at the drain (gate) was increased by a small amount. The resulting changes in the gate and drain current and voltage were computed, Fourier analyzed, and tabulated as admittance parameters. For these small signal parameters the maximum current gain (MCG) was obtained from the relation:

(10) $$MCG = 20\log_{10} |Y_{21}/Y_{11}|$$

The cutoff frequency, f_{cutoff}, occurs when MCG = 0. The maximum stable gain MSG and maximum available gain (MAG) were obtained from the expressions:

(11) $$MSG = 10\log_{10} |Y_{21}/Y_{12}|$$

(12) $$MAG = 10\log_{10} |[Y_{21}/Y_{12}][k-(k^2-1)^{1/2}]|$$

where:

(13) $$k = [2ReY_{11}ReY_{22} - Re(Y_{11}Y_{21})]/|Y_{11}Y_{21}|$$

f_{max} is obtained for MAG = 0.

III. DEVICE EQUATIONS

III.1 DRIFT AND DIFFUSION TRANSPORT

There are several descriptions of device transport that were implemented during the course of this study. The drift and diffusion equations are considered first. Drift and diffusion transport is governed by a multiplicity of electrons and holes, each separately contributing to current through the combination of a drift term, which for electrons is $-nev_n$, and a Ficks law diffusion term $eD_n\nabla n$. Here, n is the density of electrons, e the magnitude of it's charge, v_n, the electron velocity and D_n the diffusion coefficient for electrons. In combination the electron current is:

(14) $$J_n = -e[nv_n - D_n\nabla n]$$

For holes:

(15) $$J_p = +e[pv_p - D_p\nabla p]$$

each of which is constrained by continuity equations,

(16) $\partial en/\partial t - \nabla \cdot J_n = -R_n + G_n$

(17) $\partial ep/\partial t + \nabla \cdot J_p = -R_p + G_p$

in which the right hand sides express the net generation of carriers including those associated with traps, avalanching etc. Gauss's law prevails in all systems, and this is expressed as:

(18) $\nabla \cdot [\epsilon \nabla \phi] = e(n-p-C)$

where C is the net imposed background concentration, and ϵ is a spatially dependent permittivity.

Equations (14) and (15) are generally referred to as the semiconductor drift and diffusion equations. The electron and hole velocities are related to the electric field through mobility which itself may be field dependent:

(19a) $v_n = \mu_n[|\nabla \phi|]\nabla \phi$

(19b) $v_p = -\mu_p[|\nabla \phi|]\nabla \phi$

In the above expressions, the electron velocity for GaAs sustains a region of negative differential mobility which is dependent upon the ionized impurity scattering, while the hole velocity saturates without any negative differential mobility. These field dependent relations are shown in figure 2. When as assumed below, an Einstein relation is introduced for the diffusion coefficient,

(20a) $D_n = \mu_n k_b T$

(20b) $D_p = \mu_p k_b T$

the zero current, equilibrium solutions are:

(21a) $n = n_o \exp[e\phi/k_b T]$

(21b) $p = p_o \exp[-e\phi/k_b T]$

where the coefficients in front of the exponential are determined from a set of initial conditions.

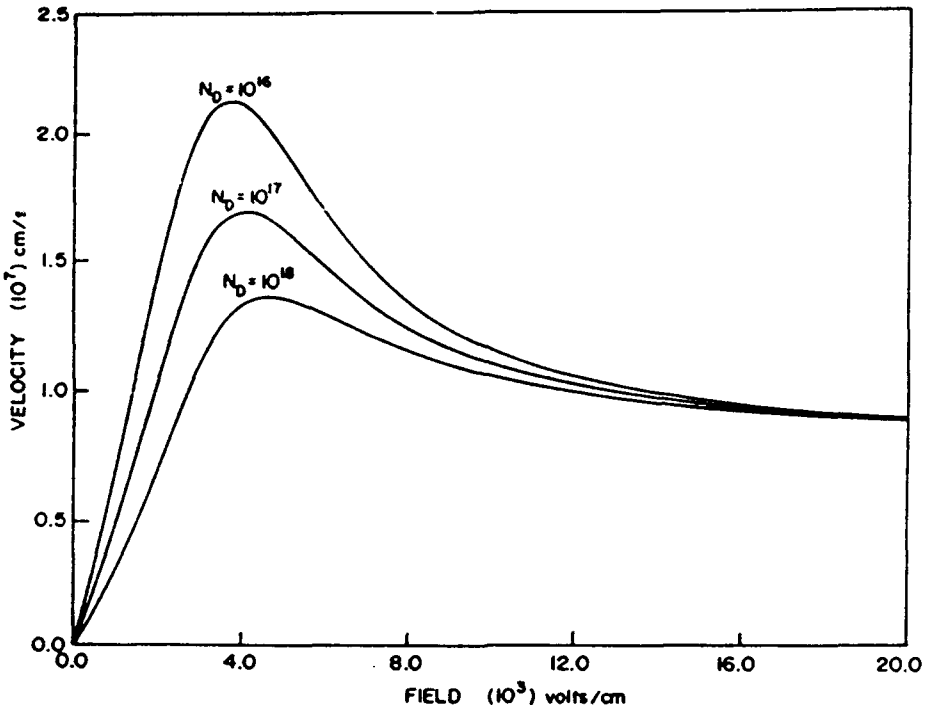


Figure 2. The field dependent velocity for electrons and holes in GaAs.

III.2 THE MOMENTS OF THE BOLTZMANN TRANSPORT EQUATION

Here, the governing equations are obtained by taking the collisional invarient moments of the Boltzmann transport equation, via., the moments with respect to the mass, momentum and energy of the carriers. This yields a set of governing equations which are similar in form to the equations utilized for multi-phase flow in fluid dynamics. The governing equations reflect the conservation laws of mass, momentum and energy for the carriers and are often referred to as the moments of the Boltzmann transport equation (MBTE).

In this study two species of electrons namely, the central and satellite valley carriers are considered. The conservation equations are:

$$\partial n_1/\partial t = -\nabla\cdot(n_1\mathbf{V}_1) - n_1 f_1 + n_2 f_2 \tag{22}$$

$$\partial n_2/\partial t = -\nabla\cdot(n_2 n\mathbf{V}_2) + n_1 f_1 - n_2 f_2 \tag{23}$$

where n_1 and n_2 are the satellite valley and central valley carrier number densities respectively while $\mathbf{V}_1$ and $\mathbf{V}_2$ are the corresponding velocities. f_1 and f_2 are the corresponding scattering integrals for particle conservation and in general are functions of the corresponding carrier temperature and momentum. For the purposes of this study, the dependence of all scattering integrals on momentum is neglected.

Conservation of momentum for the satellite valley electrons can be expressed as:

$$\partial(n_1\mathbf{P}_1)/\partial t = -\nabla\cdot(n_1\mathbf{V}_1\mathbf{P}_1) - \nabla\wp_1 - \nabla\cdot\sigma_1 - n_1 e\mathbf{F}_n - n_1\mathbf{P}_1 f_3 \tag{24}$$

where the momentum, $\wp_1$, and the field, F_n, are defined by

(25) $$P_1 = m_1 V_1$$

(26) $$F_n = -(\nabla\phi + \nabla\chi/e)$$

Here m_1 is the mass of the satellite valley carrier, e is the electronic charge, ϕ is the electric potential and χ is the electron affinity. F is the field due to potential differences and conduction band discontinuity arising from material variations. The partial pressure, $\wp_1$, is related to the satellite valley carrier temperature, T_1, and the number density by the perfect gas relationship, which results from the assumption of Boltzmann statistics,

(27) $$\wp = n_1 k T_1$$

where k is Boltzmann's constant. f_3 is the scattering integral for the satellite valley carrier momentum. The term $\nabla:\sigma_1$ represents the stress forces. In this study, the stress tensor, σ_1, is approximated by the relationship.

(28) $$\sigma_1 = \mu\nabla V_1$$

where μ_1 is the viscosity associated with the satellite valley carriers. Substitution of equation (25) and equation (26) into equation (24) yields the final form of the momentum equation for the satellite valley carriers:

(29) $$\partial(m_1 n_1 V_1)/\partial t = -\nabla\cdot(m_1 n_1 V_1 V_1) - \nabla\wp_1 - \nabla\cdot\sigma_1 + n_1 e\nabla(\phi + \chi/e) - n_1 m_1 V_1 f_3$$

It is observed that equation (29) is a vector equation and hence can in general be considered as ℓ equations where ℓ is the number of relevant physical dimensions.

Similar momentum conservation equations can be written for satellite valley electrons.

(30) $$\partial(m_2 n_2 V_2)/\partial t = -\nabla\cdot(m_2 n_2 V_2 V_2) - \nabla\wp_2 - \nabla\cdot\sigma_2 + n_2 e\nabla(\phi + \chi/e) - n_2 m_2 V_2 f_4$$

There are various forms in which the satellite valley and central valley carrier energy equations can be described. We choose to cast the energy equations in terms of the satellite and central valley temperatures, T_1 and T_2.

(31)
$$\partial(n_1 T_1)/\partial t = -\nabla\cdot(n_1 V_1 T_1) - (2/3) n_1 T_1 \nabla\cdot V_1 - (2/3k)\sigma_1:\nabla V_1 + (2/3k)\nabla\cdot(\kappa\nabla T_1)$$
$$+ 3V_1\cdot V_1 m_1[n_1(2f_3 - f_1) + n_2 f_2] - n_1 T_1 f_5 - n_2 T_2 f_6 - n_1 V_1 [T_1/m_1]\nabla(m_1)$$

Similar energy conservation equations can be written for the satellite valley electrons.

(32)
$$\partial(n_2 T_2)\partial t = -\nabla\cdot(n_2 V_2 T_2) - (2/3)\, n_2 T_2 \nabla\cdot V_2 - (2/3k)\,\sigma_2:\nabla V_2 + (2/3k)\,\nabla\cdot(\kappa\nabla T_2)$$
$$+ 3V_2\cdot V_2 m_2[n_2(2f_4 - f_2) + n_1 f_1] - n_2 T_2 f_7 + n_1 T_1 f_8 - n_2 V_2[T_2/m_2](\nabla m_2)$$

The potential is related to the total number density through Poisson's equation

(33) $$\nabla \cdot \epsilon \nabla \phi = e(n_1 + n_2 - n_0)$$

where n_0 is the donor density, and ϵ is the permitivity.

In two dimensions, the complete problem description requires 9 equations consisting of 2 continuity equations, 4 momentum equations, 2 energy equations and a Poisson's equations. The boundary conditions for potential are the same as we used for the drift and diffusion equations. At ohmic contacts, the boundary condition is given by the sum of the applied bias and an appropriate built-in potential. The temperature of all carriers are assumed to be at 300k at the ohmic contacts. The carrier densities at the contacts are fixed at the value of local doping. For velocities, the normal gradient is taken to be zero.

IV. DEVICE SIMULATIONS

Three broad classes of structures were examined during the course of the study: the permeable base transistor, vertical structures as represented by heterostructure bipolar transistors, and the opposed source gate transistor.

IV.1 THE PERMEABLE BASE TRANSISTOR

The first structure studied, and indeed the one to which most of the large signal concepts were tested was the permeable base transistor. A detailed discussion of the PBT is not warranted here as it has been presented before.

Prior to any rf testing of these structures, dc characterization takes place. In collaboration with the workers at Lincoln Laboratories several structures were studied with the goal of determining which of these structures sustained the highest voltage prior to breakdown. These breakdown calculations were the first to be performed for the permeable base transistor. For this study three types of PBTs were studied, each with a different doping profile. These structures are shown in figure 3. The first, structure A, is the one typically studied. It consists of a uniform doping profile with a tungsten gate at one side of the structure. Structure B mimics a space charge injection profile, in which the active region is confined to the narrow 2000Å surrounding the base of the device. Structure C is one in which the region surrounding the base is more heavily doped.

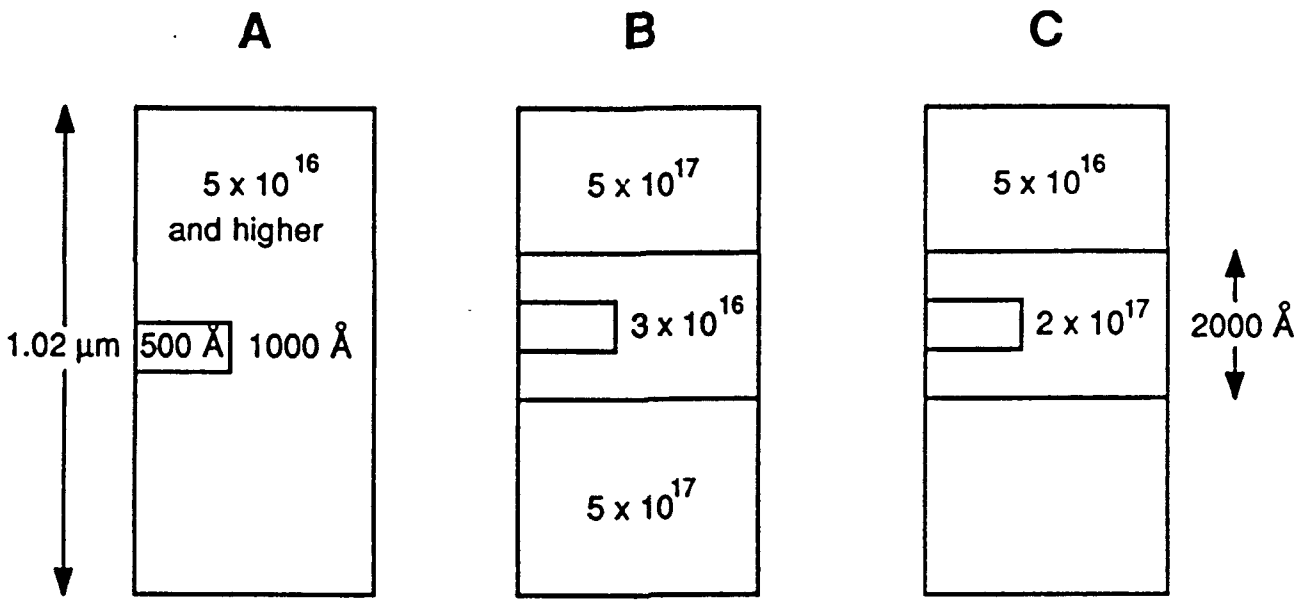


Figure 3. Schematic representation of the types of PBT structures studied during the course of the Contract. The structures are not to scale. Variations of each are discussed in the text.

THE DC CHARACTERISTICS

The dc current voltage characteristics of device A are shown in figure 4 and display breakdown voltages of nearly 20v at a forward bias of 0.4v on the base. The breakdown voltage at zero and reverse bias on the gate is expected to be higher although it was not calculated. This high breakdown voltage is rather remarkable in light of the 5 to 7 volt breakdown voltages common to GaAs FETs.

The origin of the high breakdown voltage lies in the distribution of potential, and thus in the design of the PBT. This conclusion is a result of parametric studies and is best illustrated by the studies of structure B. Unlike structure A, structure B must be regarded as a submicron PBT in that the primary active region is restricted to the low doped region. Thus while for uniformly doped PBTs, most of the channel potential drop is in the vicinity of the base region, pushing the collector closer to base results in a considerable alteration of the potential distribution.

Consider, for example structures B1, B2 and B3. For structure B1, (figure 5) the base contact is centrally placed, and the base width is 300Å. The width of the low doped region is 3300Å. For a forward bias 0.4v on the base, the current voltage characteristics are displayed in figure 5. Notice that the breakdown voltage is approximately 12 volts, which is considerably lower than that of structure A. To develop some understanding of this result two additional calculations were performed. One for a structure in which the distance between the base contact and the collector region was reduced to 1000Å, structure B2, and a second, in which the distance between the base contact and emitter was reduced to 1000Å. The results are displayed in figures 6 and 7, where it is noticed that the lowest breakdown of all is that for the structure in which the base-collector separation is smallest.

The distribution of potential for the forward bias of 0.4v on the base contact is displayed in

figures 8 and 9, for two different values of collector bias. Note that the potential drop, which is the same for both structures, falls over a shorter distance for the structure in which the collector region is closer to the bear contact; thus the electric field is higher in the

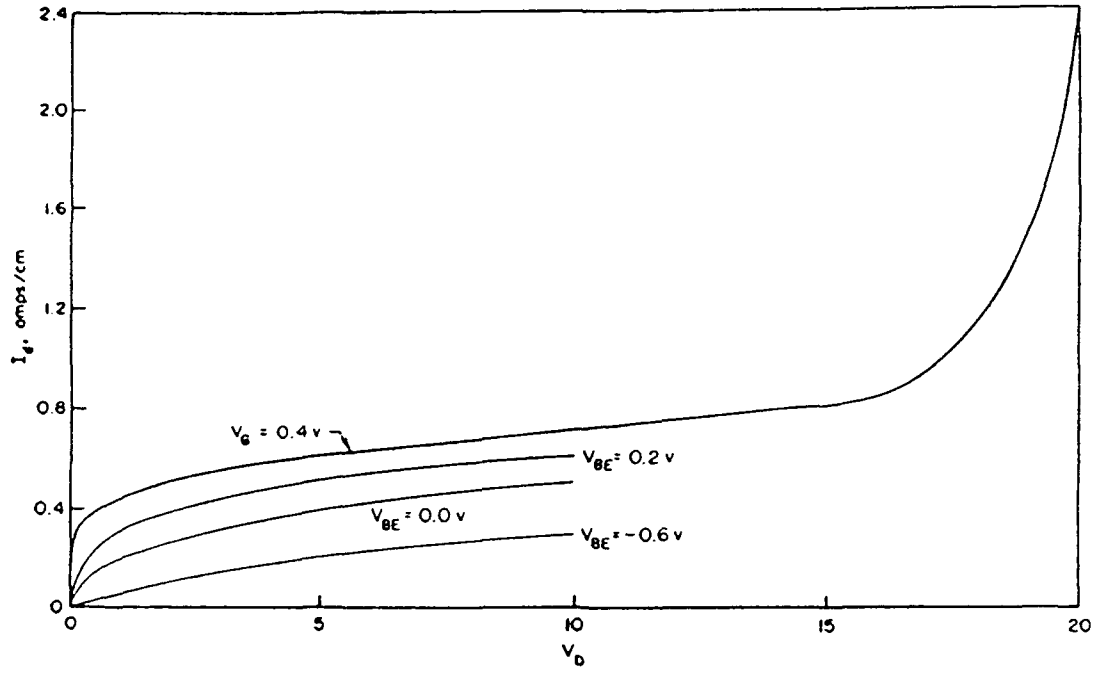


Figure 4. DC current voltage characteristics of the PBT with structure A. Breakdown calculations were performed only for the forward bias of 0.4v.

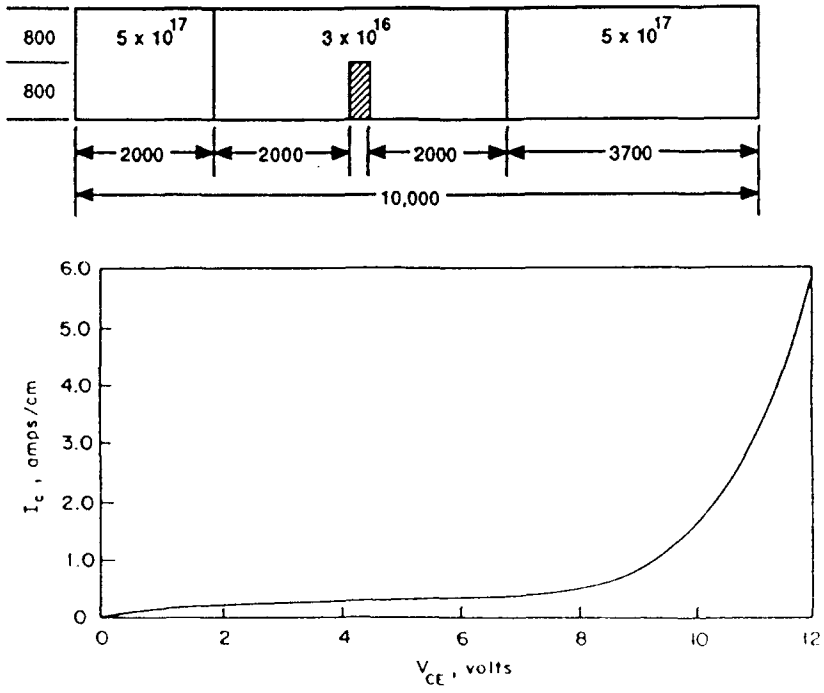


Figure 5. Structure and DC current-voltage characteristics of the PBT, structure B1, at a forward bias of 0.4v.

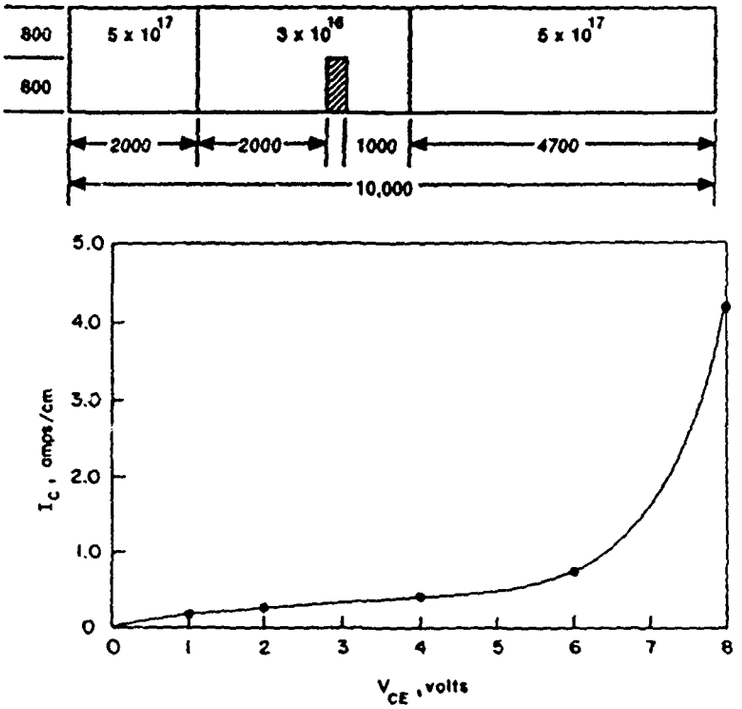


Figure 6. Structure and DC current-voltage characteristics of the PBT, structure B2, at a forward bias of 0.4v.

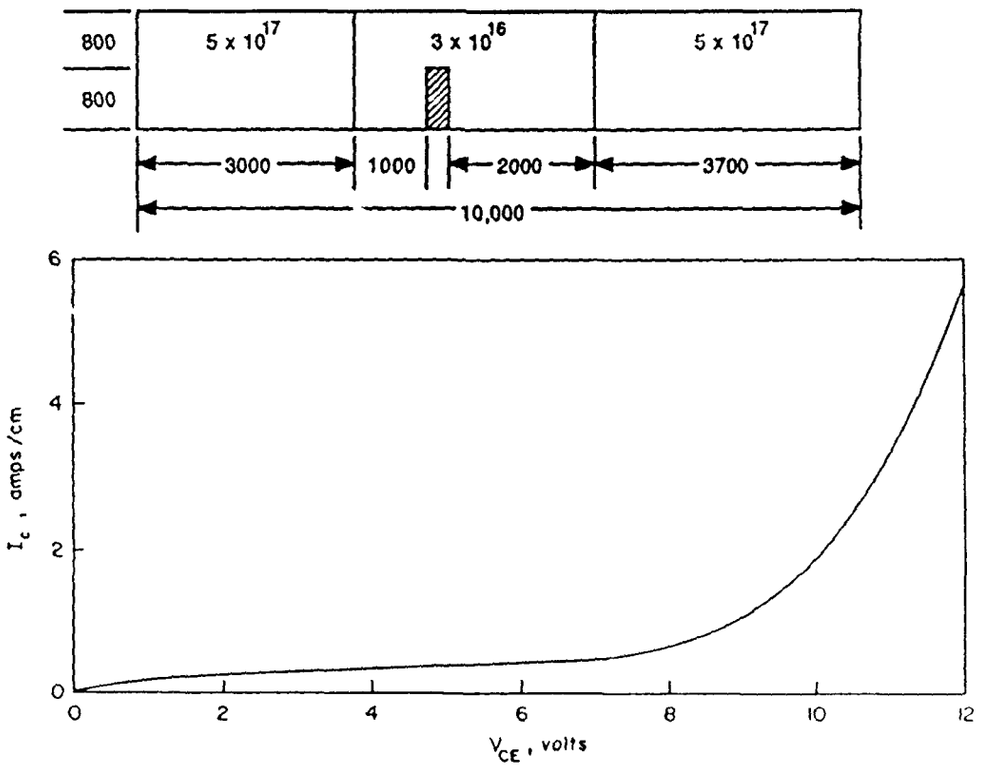


Figure 7. Structure and DC current-voltage characteristics of the PBT, structure B3, at a forward bias of 0.4v.

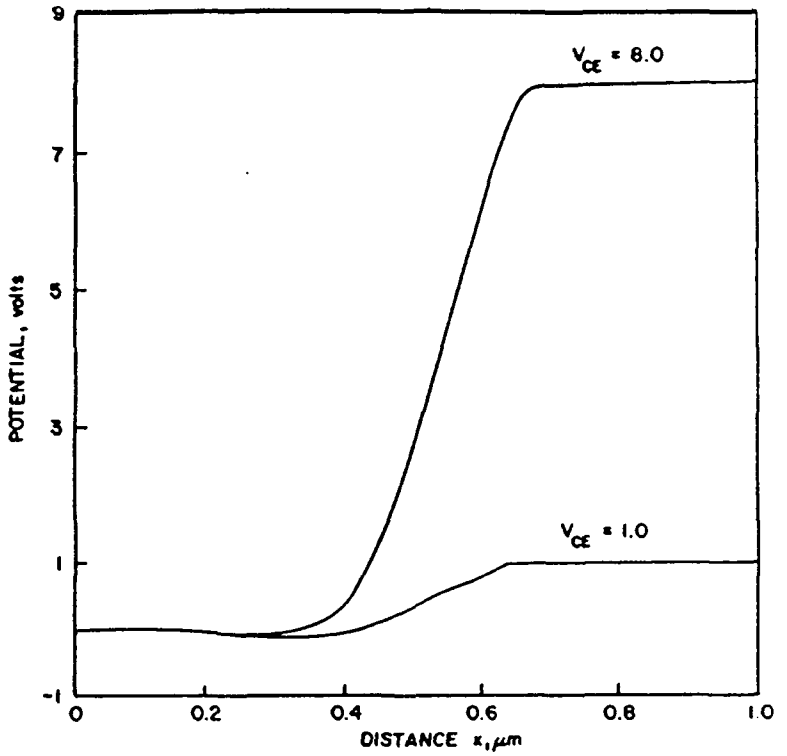


Figure 8. Distribution of potential along the center of the channel for the PBT structure B1 at a forward bias of 0.4v.

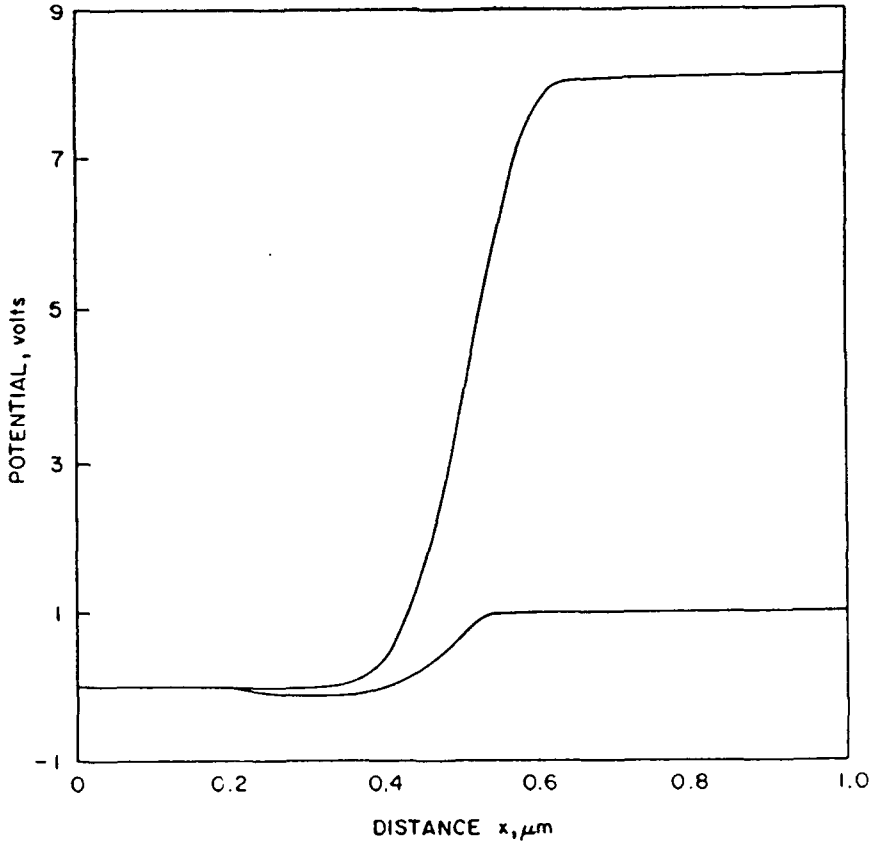


Figure 9. Distribution of potential along the channel for the PBT structure B2, at a forward bias of 0.4v.

structure with the shorter base collector region. In the model calculations performed, breakdown occurs at a threshold field; thus breakdown would occur at lower voltages for the smaller base collector spacing. It must be cautioned that this result is model dependent. Breakdown does not occur when the field reaches a specific value, but when the carriers are sufficiently energetic to strip the ions of carriers. Thus in a more realistic calculation the differences between the results of structures like that of B1 and B2 may not be as great as that depicted in the above figures.

The DC electrical characteristics of the PBT with the heavily doped base region are shown in figure 10, for a collector voltage up to 3.0v, and in figure 11 for a collector voltage to 18v. It is seen that the current levels are approximately the same as the uniformly doped structure, as is the breakdown characteristic. The higher breakdown voltage is not unexpected, as the low doped collector region does not have as strong an impact on restricting the voltage distribution as does the heavily doped collector regions.

There is an interesting point that should be emphasized at this juncture, and it emerges from a cursory examinations of the dc characteristics of the PBT devices A and C. These characteristics are not dramatically different, yet the physical structures are different. Thus additional characterization is needed. In this matter we can look at the small signal characterization, although we bear in mind that we are interested in the large signal behavior of the PBT.

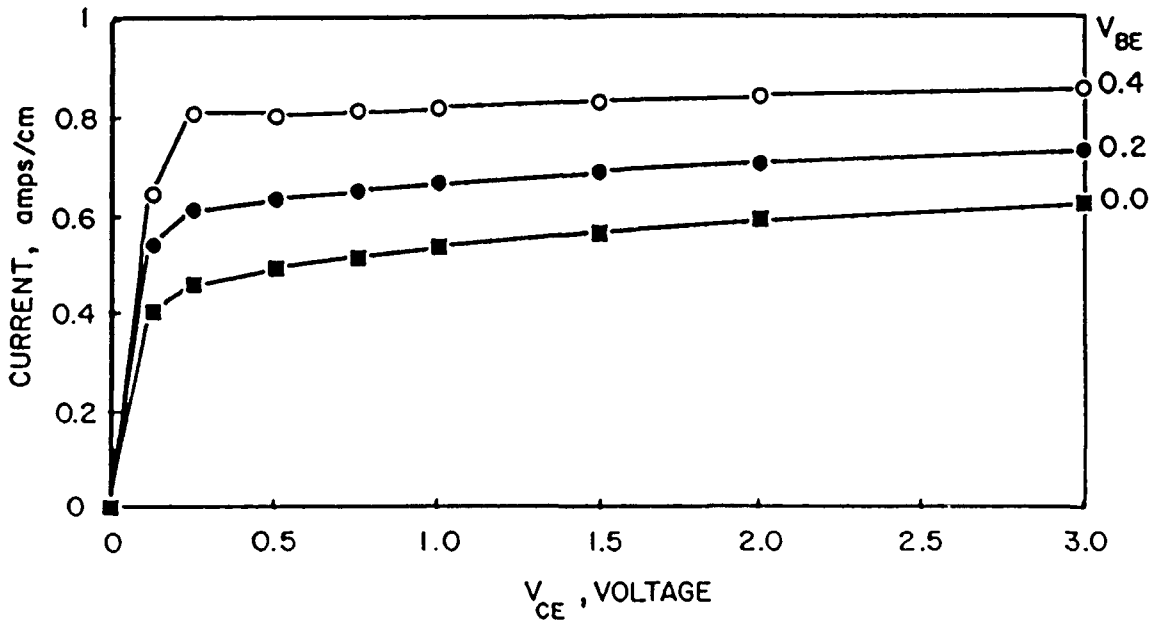


Figure 10. DC current voltage characteristics for the PBT structure C

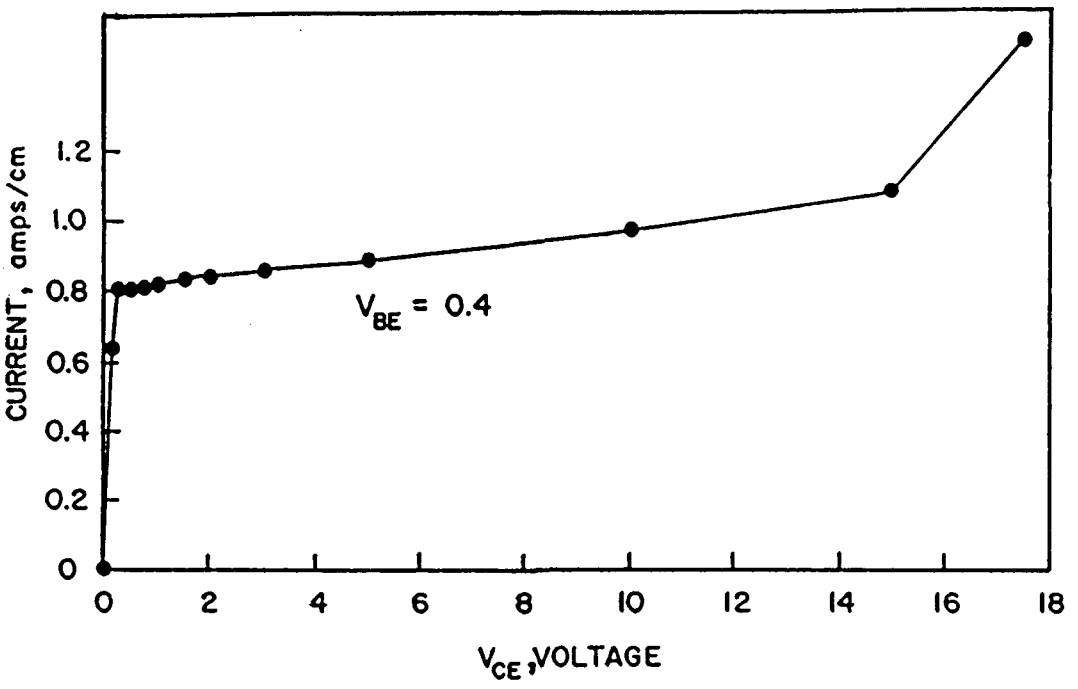


Figure 11. DC current voltage characteristics for the PBT structure C, carried to breakdown.

One of the most commonly used figures of merit for the operation of three terminal devices is the cutoff frequency, f_t. We have used several ways of calculating f_t. One is through the formula: $f_t = g_m/[2\pi C_{gs}]$, where g_m is the dc transconductance and C_{gs} is the gate-source capacitance. Another is to determine the frequency at which MCG, given by equation (10), is zero. Both yield the same answer. There are several key features that affect the cutoff frequency: (a) increases in carrier density increase the cutoff frequency, (b) and decreases in base width increase the cutoff frequency. Figure 12 displays the cutoff frequency versus base-emitter voltage for PBT structure A, with different densities, as well as different base widths. The calculations were performed for a half-channel opening of 1000Å, and a collector-emitter voltage of 1.0v. Note that the cutoff frequency approaches 42GHz for the highest density and smallest base-width structure.

The maximum current gain, as computed from equation 10, is displayed in figure 13 for two different structures, device A at higher bias levels, and device B3 at the indicated bias levels. Several points are noteworthy. The first point is that the cutoff frequency decreases with increasing collector bias, a result obtained by others. The second point is that the cutoff frequency is less for the lower doped device B3, in comparison to the device A, but that the degradation of cutoff frequency for device B3 is negligible compared to device A.

The situation with the PBT with the higher doping surrounding the base contact is displayed in figure 14. As anticipated the cutoff frequency is highest for this structure, as it has the higher doping surrounding the base contact. Unfortunately the degradation of cutoff frequency with bias is severe for this structure.

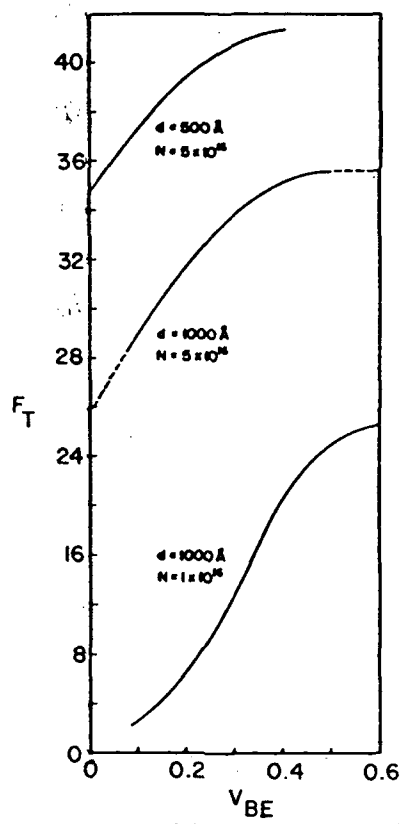


Figure 12. Cutoff frequency versus base-width and nominal background doping, for the PBT structure A. The channel half-opening is 1000Å, and the collector voltage is 1.0v.

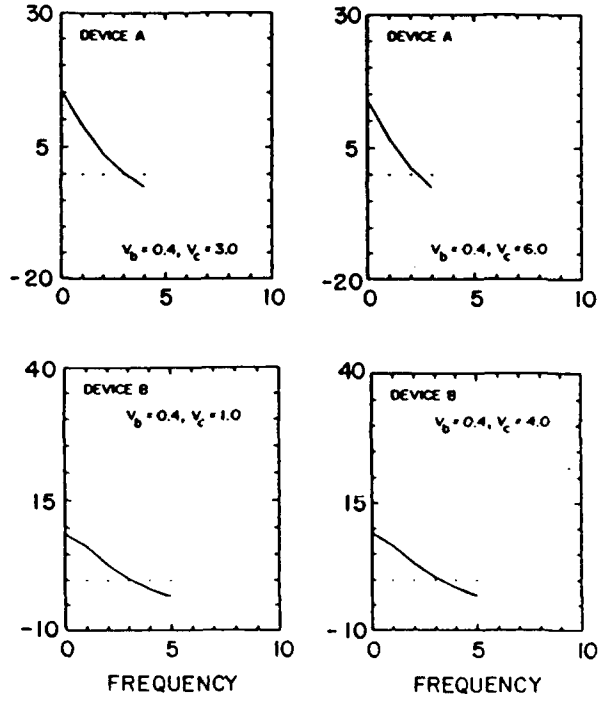


Figure 13. Maximum current gain, as computed from equation (10), For PBT structure A, at higher bias levels, and for PBT structure B2.

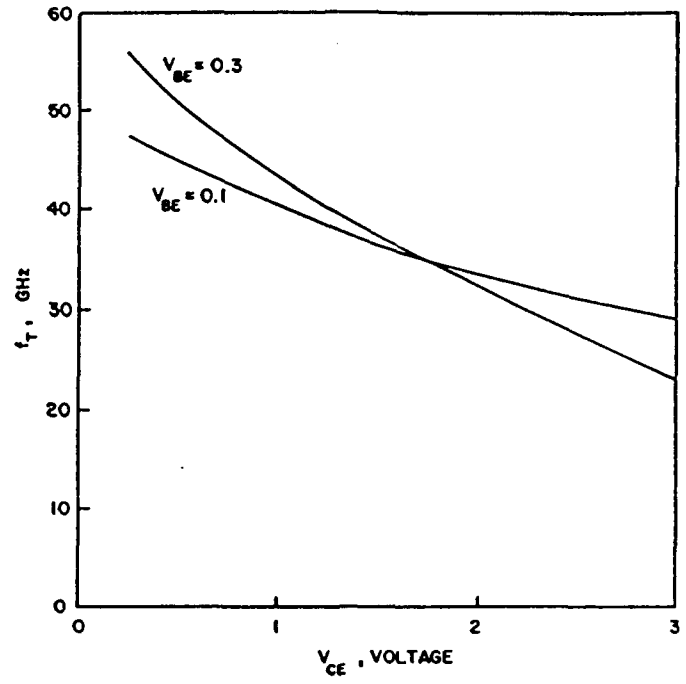


Figure 14. Cut-off frequency for PBT device C.

LARGE SIGNAL PBT CALCULATIONS

As discussed in the introduction, the evaluation of the potential performance of semiconductor devices for analog applications has heretofore been approached through two distinct processes: (i) small signal characterization as obtained from admittance or scattering calculations, or (ii) the application of large signal ordinary differential equation representations of devices coupled to their respective linear circuit representations. There has however, very recently been some generalizations of this approach, see e.g. [1]. In addition further advances involve coupling the ODE representation of the device to a complex embedded multiple element array.

The above approaches are very weak, particularly when high frequencies are needed. To expose this weakness we first concentrate on the issue of small signal characterization as a basis for the large signal performance of devices. In discussing this we point out that for large signal operation, the base and collector voltages will normally undergo large swings, constrained by a load line. Thus a typical calculation may involve swings between the knee of the PBT IV characteristic and breakdown. Consider therefore figure 15, which displays the steady state distribution of charge for the PBT structure A at two extreme values of voltage pairs. It is noticed that the contours of density show extreme differences at these bias levels, leading one to be suspicious of the small signal characterization as a reasonable representation of the large signal device behavior. It should be pointed out however, that if calculations are limited to small changes in collector voltage, the application of small signal parameters may be more satisfactory. This argument is supported by the calculations of figure 16, which show density contours at the same value of collector voltage, but at different values of base voltage. While there are differences in the contours, these results are not as dramatic as those shown in figure 15.

The situation becomes even more dramatic when we consider the fact that as the frequency

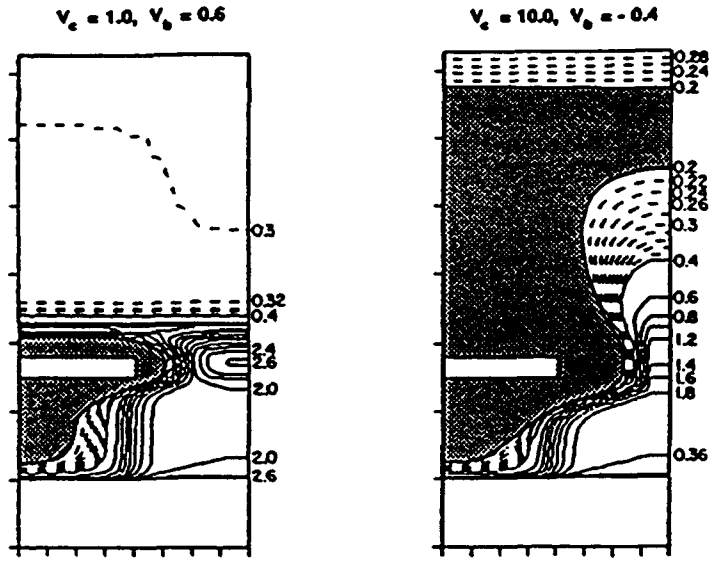


Figure 15. Contours of carrier density for the PBT structure A at two extreme values of base and collector voltage levels.

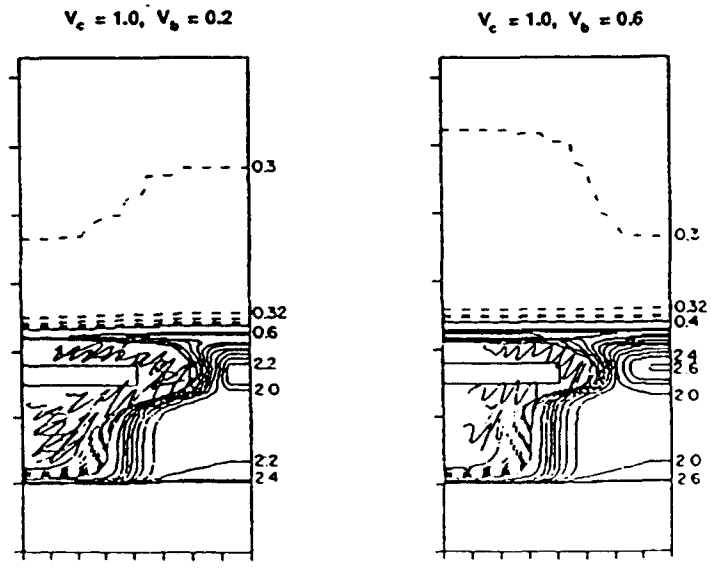


Figure 16. Contours of density for the PBT structure A, at the same value of collector voltage, but different values of base voltage.

increases the carrier response to changes in device voltage, which is never instantaneous, will have a greater impact on device performance.

To begin to examine the large signal characteristics of the structure consider figure 17, which is a schematic of the dc characteristics of the PBT, through which a dc load line is drawn. The imposition of a sinusoidal voltage on the base contact results, at low frequencies in an ac voltage on the collector contact. Because of the dc load line the net power delivered to the load is $I_A V_A/2$, where I_A and V_A are respectively the amplitudes of the current and voltage at the collector contact.

The construction of figure 17 teaches that under dc conditions and for a resistive load attached to the collector contact, a specified value of base voltage will lead to a unique value of collector voltage. Under time dependent conditions this is no longer the case. In particular, the application of an ac voltage to the base contact will necessarily result in capacitive currents, whose magnitude increases as the frequency increases. These capacitive current contributions are in part affected by the transient movement of charge within the structure, and as a consequence a unique value of base voltage no longer leads to a unique value of collector voltage. The capacitive contributions lead to 'looping' or hysterisis in the relation between the base and collector voltages as shown in figure 18 for a time dependent voltage on the base of $V_b = 0.0 + 0.4\sin\omega t$.

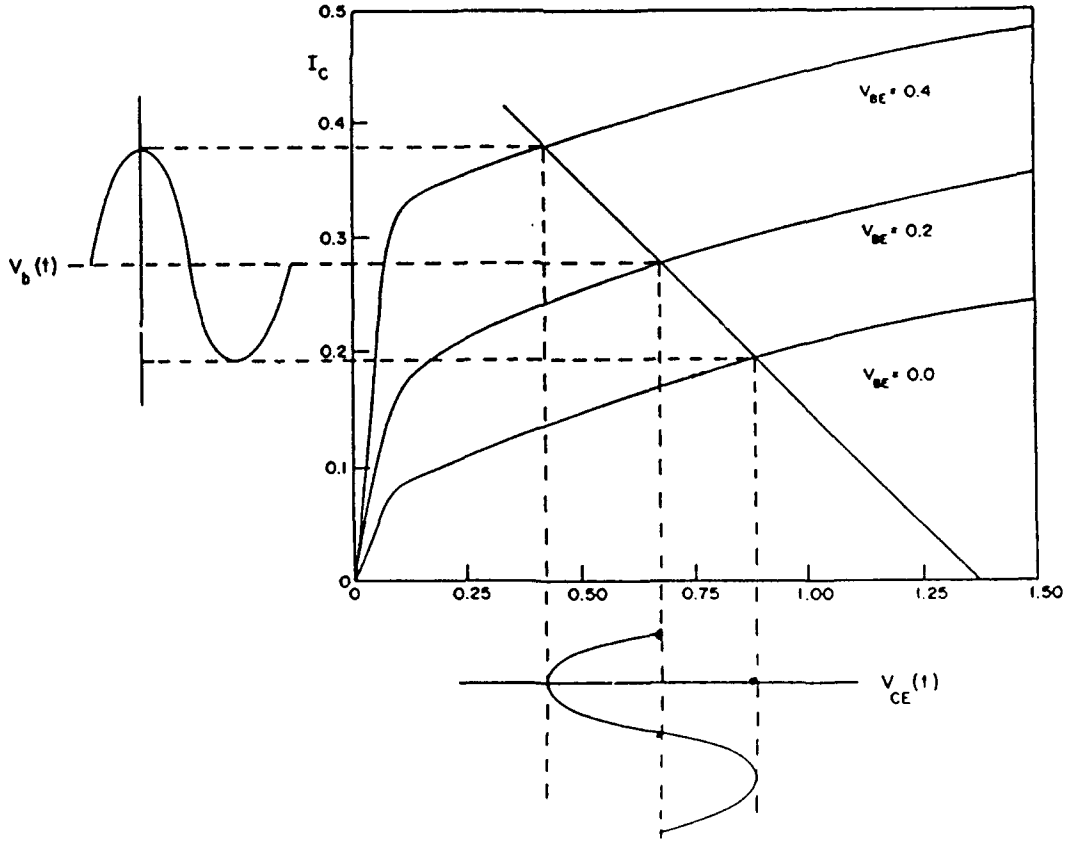


Figure 17. DC analysis of the voltage variations at the collector contact for an imposed bias on the base contact.

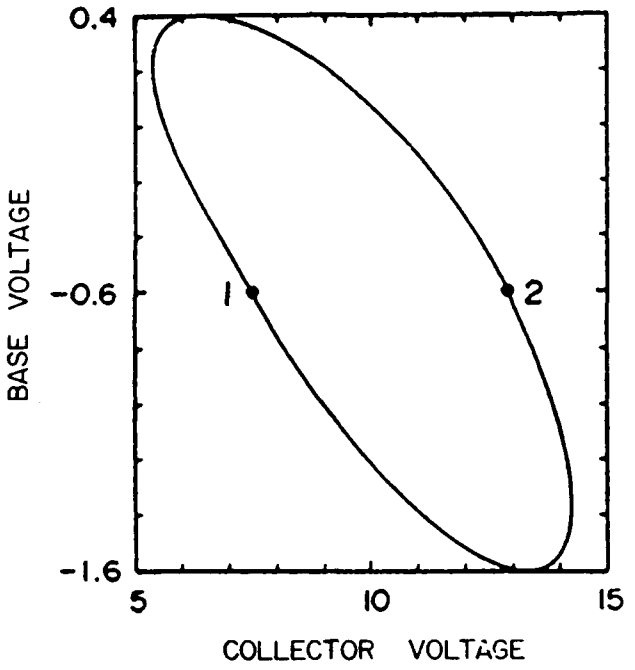


Figure 18. Lissajous of the base and collector voltage for the PBT structure A subject to a base voltage of $V_b = -0.6 + 1.0\sin\omega t$. The frequency for this oscillation is 40GHz.

The way the above results and those below are obtained is as follows. The boundary condition on the base contact is:

(34) $$V_b = V_b(0) + \delta V_g \sin\omega t$$

where $V_b(0)$ is the quiescent bias or dc bias point. δV_b is the amplitude of the imposed sinusoidal base voltage. The time dependent boundary conditions on the collector contact are obtained from the ordinary differential equations governing the circuit attached to the collector loop. For example, in the simplest case of a resistive circuit,

(35) $$V_c = V_{BT} - I_o(t)R$$

where V_{BT} is the bias connected to the collector through the load, $I_c(t)$ is the collector current and R is the resisitive collector load. When the collector loop was composed of a simple reactive circuit, such as that shown in figure 1, the choice of circuit inductance and circuit capacitance arbitrarily set the constraint that the reactive circuit have a natural frequency f_r that was a fractional or multiple harmonic of the base driving frequency. The natural frequency of the reactive collector circuit is:

(36) $$f_r = [1/2\pi LC]^{1/2}$$

In many of the calculations discussed below f_r is fixed while values of L and C are varied. This has the effect of altering the Q and phase of the circuit. Several definitions are in order. The unloaded Q of the resonant circuit in figure 1 is

(37) $Q_u = \omega_r RC$

where $\omega_r = 2\pi f_r$; the unloaded Q is a measure of the ratio of the energy stored in the resonant circuit to the power loss in the resonant circuit. There is also the loaded Q, which is a measure of the ratio of the energy stored in the resonant circuit to the total power loss in the system.

To understand the result symbolized by figure 18, we examine some of the details of the calculation. The dc IV characteristics of structure A for which the large signal calculations were performed are shown in figure 4. For the large signal calculations the dc collector resistance was chosen such that the collector current was zero at a collector voltage of 20v, and a collector current of 0.3amp/cm at a zero value of collector voltage.

The time dependent terminal characteristics, when a sinusoidal voltage is applied to the base of the PBT is shown in figure 19 (the current is in multiples of 2.4amps/cm) for a full PBT cell subject to a base voltage of $V_b = -0.6 + 1.0\sin\omega t$. The imposed base frequency is 40 GHz, while $f_r = 60$Ghz. The values of L and C are indicated in the subsequent diagrams. Note that an initial transient is followed by a steady state periodic 40GHz oscillation. For this oscillation the collector current becomes slightly negative indicating class B operation. The terminal characteristics are a consequence of simultaneous solutions to the drift and diffusion equations and the external circuit equation and reflect the transient not the steady state time independent charge distribution within the PBT, as demonstrated in figure 20.

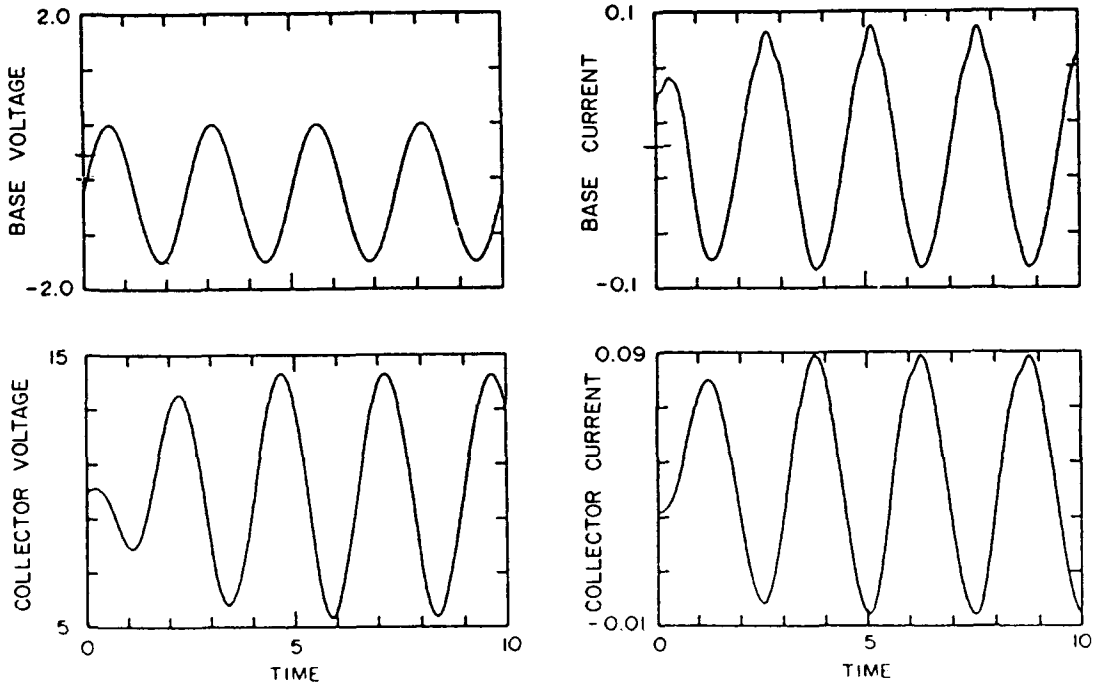


Figure 19. Time dependent current and voltage through the base and collector for $V_b = -0.6 + 1.0\sin\omega t$. The driving frequency is 40 GHz, $f_r = 60$ GHz, $C = 5.10\times10^{-16}$ farads and $L = 1.38\times10^{-8}$ henries.

Figure 20 displays a repeat of the lissajous of figure 18. In addition contours of carrier density and potential are shown at two different times during the oscillation, but at the same value of base voltage. (In this figure the emitter and base contacts are at the bottom and left of the structure, respectively. Voltage contours are in multiples of volts, while density contours are in multiples of $5x10^{16}/cm^3$.) Noting that the net depletion under the base contact is a consequence of both the base and collector voltage, it is seen that the extent of the depleted zones is different for the same value of base voltage. For example at point '1' on the lissajous the field under the base contact is lower than that corresponding to the point '2' on the lissajous. This result also appears in studies at other bias levels and other frequencies. The second point we note is that the density contours display an excess, or accumulation, of charge under the base contact at both lissajous points '1' and '2', but that the accumulated charge is greater at lissajous point '2'. This increased accumulation layer is also accompanied by a broad depletion layer between the base and collector region. It is clear from these figures that the transient operation of the PBT is governed by the detailed transient behavior of the charge distributions and that the steady state solutions, which will yield different distributions of charge than those shown in the transient figures, and not be used with any degree of confidence in designing PBT devices. Very similar conclusions were arrived at for more classical types of transistors, such as the GaAs FET, and have been reported elsewhere.

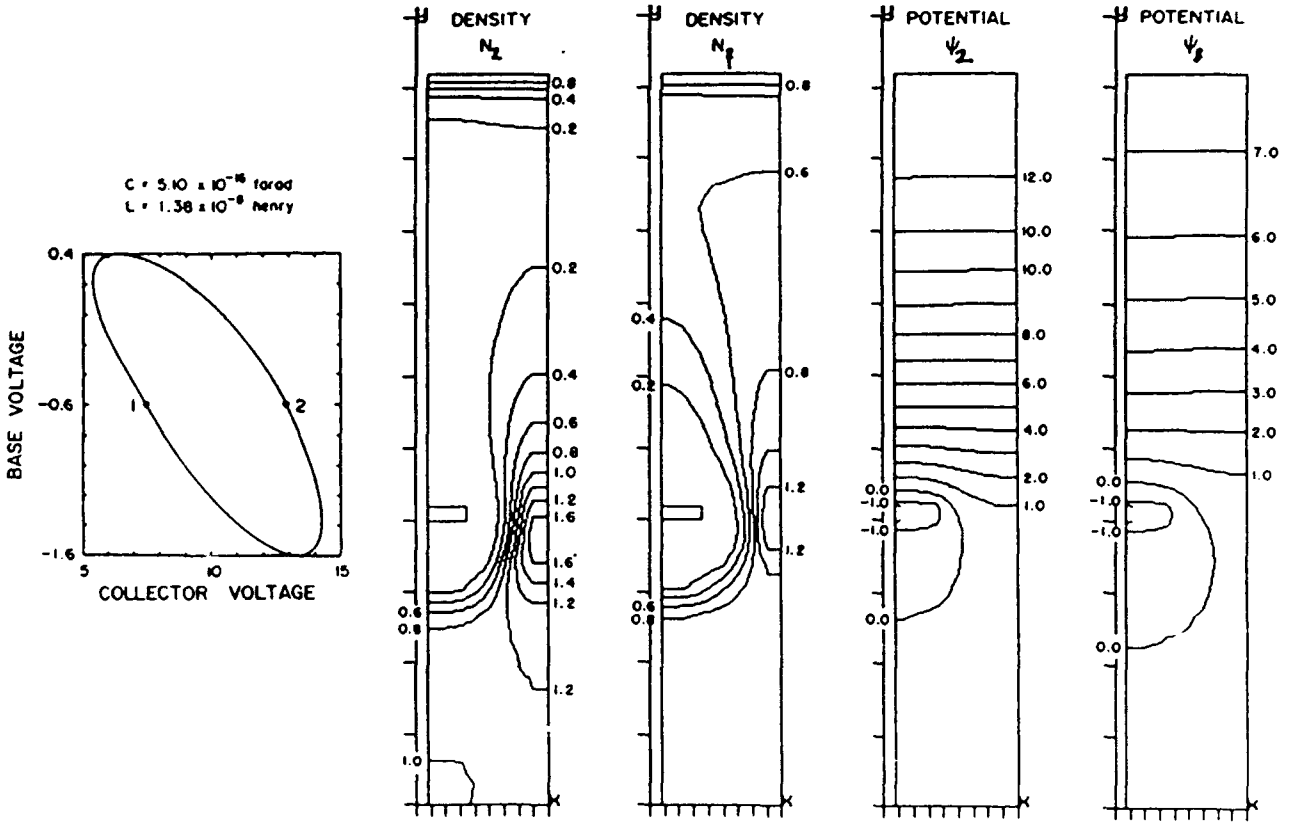


Figure 20. Density and potential contours for two different transient pairs of base and collector voltage, corresponding to the parameters associated with figure 19.

LISSAJOUS FIGURES....RESISTIVE COLLECTOR CIRCUIT CALCULATIONS

The above discussion establishes the principles associated with the large signal calculations. It is important to backtrack for a moment and establish that the phase relationships between the base and collector voltages, reflect contributions due to the external circuit, and the internal transient dynamics of the carriers,with the latter dominating. We demonstrate this by attaching a dc load to the collector contact, and assume all time dependent external driving voltages are associated with the base contact. The time dependence associated with the collector contact is that arising from the simultaneous solutions of the drift and diffusion equations and the resistive circuit equations.

The calculations we discuss there are those displayed in figure 21. Here for a dc bias on the collector contact of 10volts, and a base voltage of $0.1\sin\omega t$, $0.2\sin\omega t$, and $0.6\sin\omega t$, where the driving base frequency is 20GHz, 40GHz and 60GHz, the base-collector voltage lissajous shows a progressive change in the direction of the major axis. For example, at the low 20GHz frequency, the slope of the base-collector major axis is similar to that of the dc load line, as in the case of figure 20, although in the latter the slope receives important contributions from the external circuit, as discussed, below. However, as the circuit frequency increases, the electrons do not respond as rapidly to changing voltages, relative to their response time at lower frequencies, and the slope is altered by almost 90 degrees.

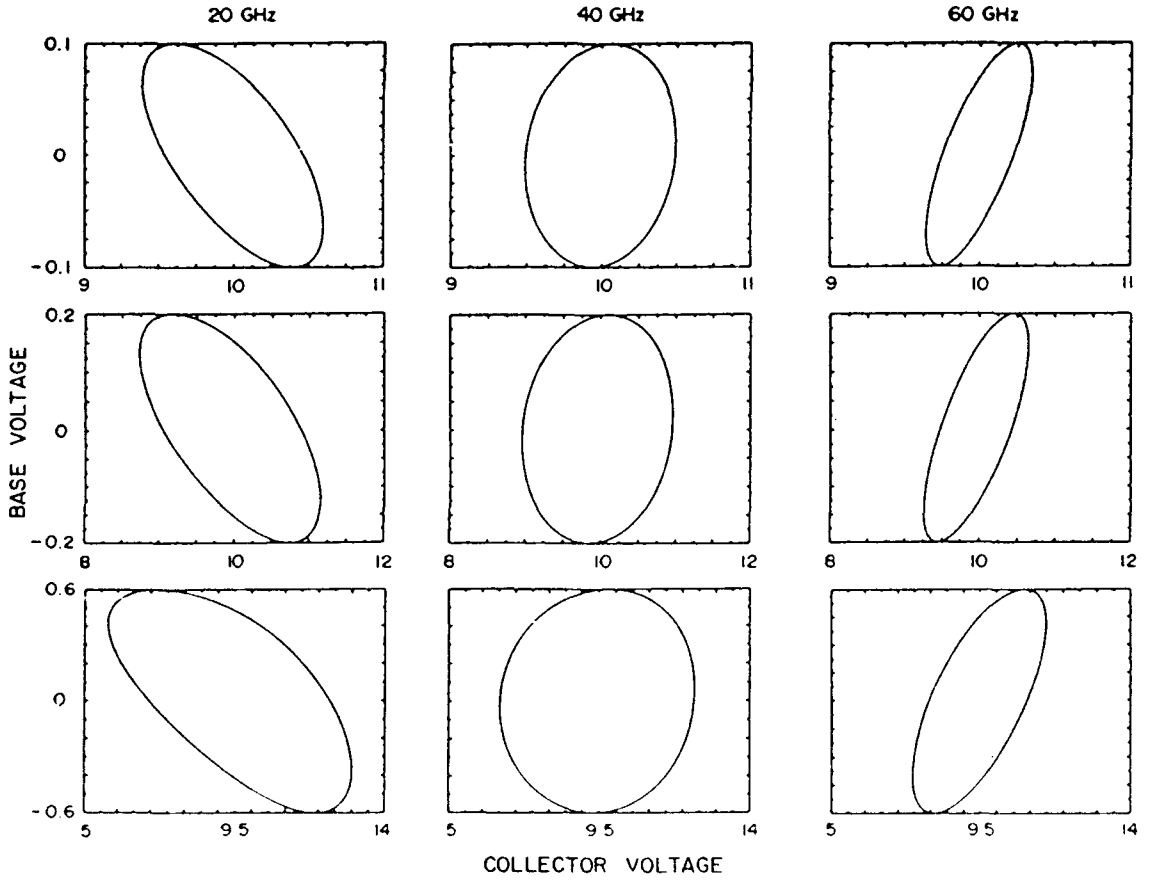


Figure 21. Base-collector voltage lissajous for a driving sinusoidal base voltage and a resistive collector load line. The nominal collector voltage is 10v.

Now while it may be argued that an equivalent circuit representation of the PBT can be designed to yield the same results as those in figure 21, there is no reason to do this other than to speed up computations at a designers workstation. The results of figure 21 display the important device physics associated with the carrier response time. There is another point to note. Each row of figure 21 corresponds to an increasing value of base voltage swing. The top row corresponds to a base amplitude of 0.1 volts while the bottom row corresponds to a base amplitude of 0.6 volts. There is a corresponding increase in the amplitude of the collector voltage. For example, at 20 GHz, the amplitude of the collector voltage is approximately 0.6 volts for a base amplitude of 0.1 volts, while it is approximately 4.0 volts for a base amplitude of 0.6 volts. At 60 GHz, the collector amplitude, apart from the phase difference, is reduced to approximately 0.4 volts for the base amplitude of 0.1 volts, while for a base amplitude of 0.6 volts the collector amplitude is reduced to approximately 1.5 volts. Thus for the resistive circuit the frequency variation is expected to have a significant effect on the power gain of the structure. Indeed as the frequency increases the power gain should decrease, and the origin of this lies in frequency response of the carriers.

The large signal power gain is defined as follows:

(38) $$LSG = 10\log_{10}|LSPA|$$

where LSPA is the ratio of equation (9) to equation (8). The letters 'LS' denote large

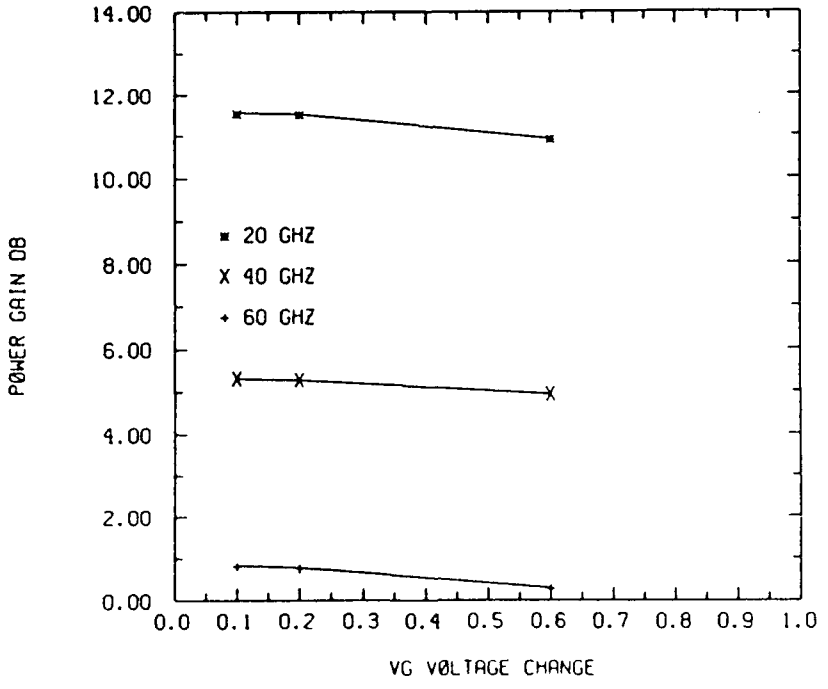


Figure 22. Large signal power gain (db) as a function of the amplitude of the base voltage and the driving base frequency.

signal. Figure 22 displays the anticipated reduction in power gain as the frequency is increased. Note there is only a small decrease in power gain as the amplitude of the base voltage increases.

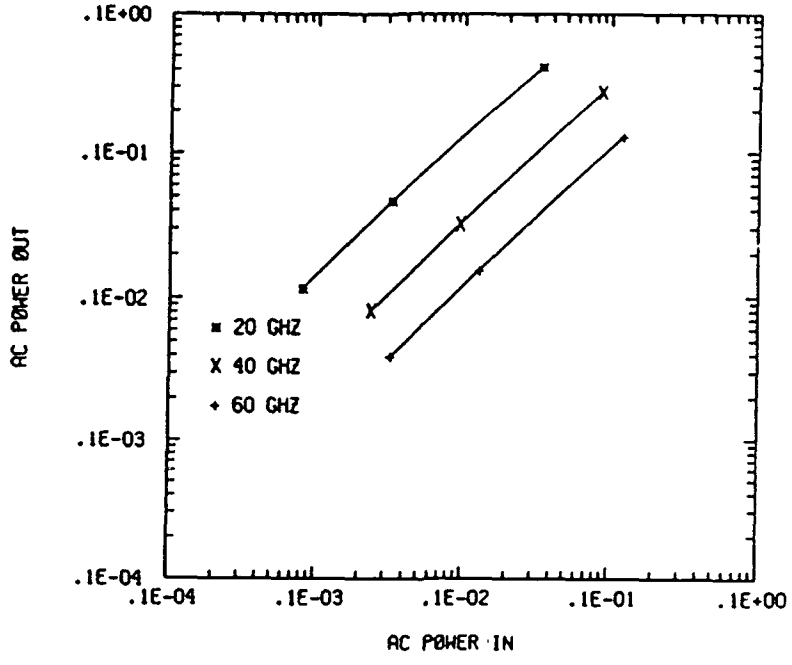


Figure 23. AC output power versus AC input power for structure A.

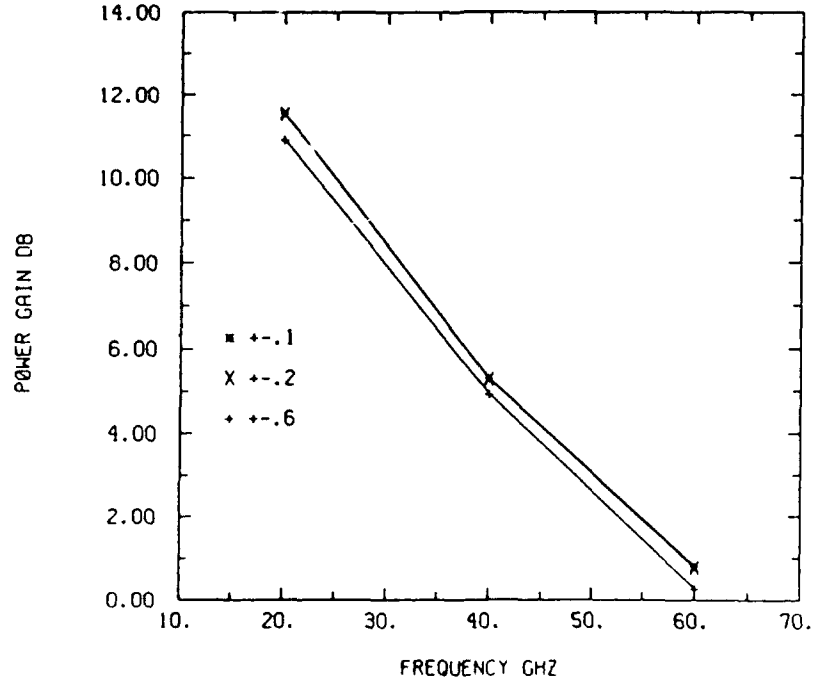


Figure 24. AC power gain as a function of frequency for structure A.

The gain for this structure is approximately linear over the bias ranges chosen as is revealed in figure 23, which displays AC output power versus AC input power as a function of frequency. The output power gain as a function of frequency is displayed in figure 24, where it is seen that for the range of voltages chosen the power gain is relatively independent of the amplitude of the base voltage.

The calculations discussed above have concentrated primarily on the amplitude and phase of the base and collector voltages. Clearly there are other lissajous structures. For the situation we have been discussing where the load is resistive the drain current and drain voltage lissajous is linear and represents a straight line, as indicated in figure 25. If we were to anticipate what the base current and base voltage lissajous would be we would conclude that if the current through the base contact were entirely capacitive, then depending on the

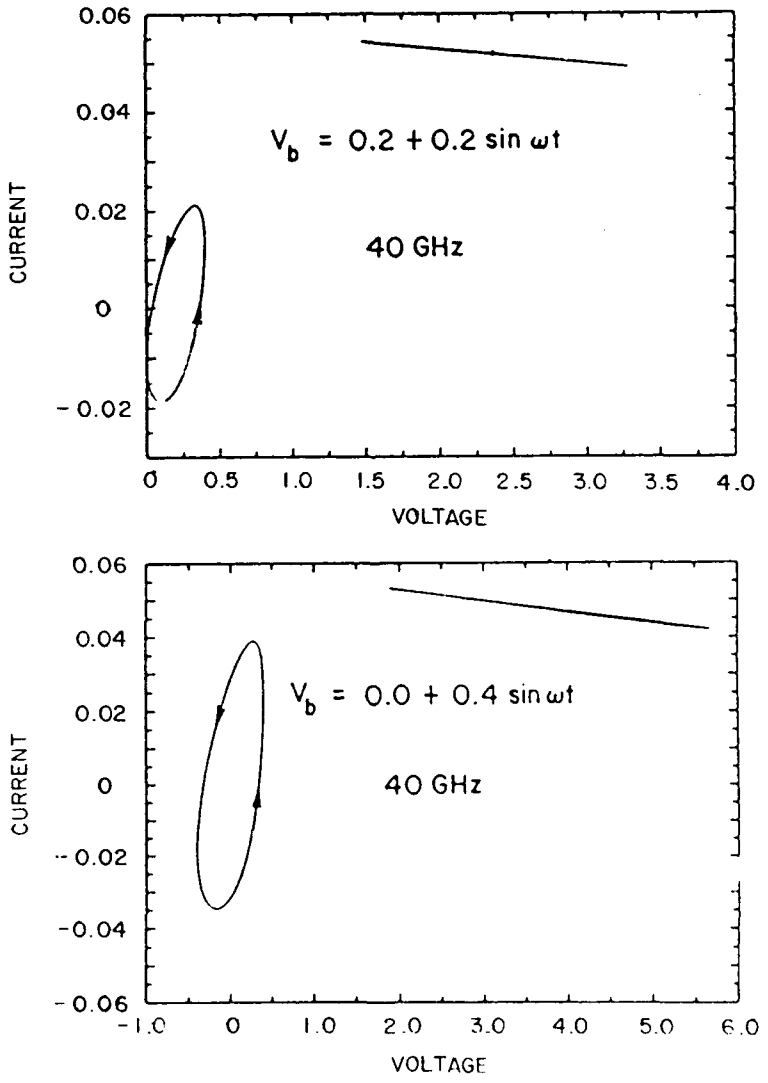


Figure 25. Base current-voltage lissajous and drain current-voltage lissajous for the PBT structure A at a driving frequency of 40GHz and varying set points in voltage.

scale of the axes, the lissajous would either be a circle or an ellipse (with axes parallel to the abscissa or ordinate). This is not the case as displayed in figure 25 for a 40Ghz driving frequency. Of particular interest is the slope of the base current-voltage lissajous, and the squashing of the characteristic at high base current and voltage. This result strongly implies that transport associated with the base contact is considerably richer than that associated solely with capacitive contributions.

LISSAJOUS FIGURES...REACTIVE COLLECTOR CIRCUIT CALCULATIONS

With the exception of the discussion associated with figures 18 through 20, which introduced the large signal calculations, the previous discussion has involved only the presence of a resistor in the collector loop. The discussion that follows illustrates the role of the reactive element on the operation of the PBT.

Figure 26 displays the base-collector voltage lissajous for structure A with a zero dc base dc voltage of 0.0v, an ac amplitude of 0.2volts and a driving gate frequency of 40GHz. The four frames of figure 26 correspond to calculations with circuit elements with the indicated value. The natural resonant frequency associated with each of these elements is indicated. Note that the slope of the gate drain lissajous is dependent upon relative values of the circuit and drive frequency.

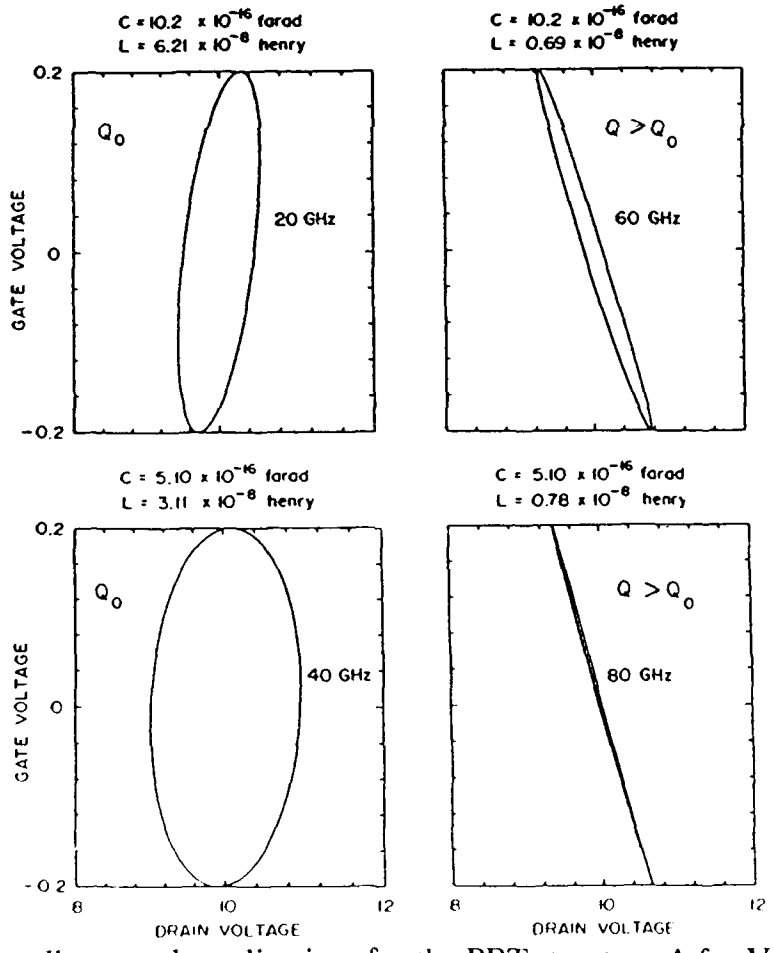


Figure 26. Base-collector voltage lissajous for the PBT structure A for $V_b(0) = 0.0v$. $\delta V_b = 0.2v$, $f = 40GHz$, and f_r as indicated.

The shape and slope of the lissajous figures is being emphasized because of the possible role they may play in the design of actual transistors. The key issue with these structures is the gain, etc. Power calculations were performed for the simulations of figure 26. In order of increasing frequency the power gain (total) were respectively 1.6dB, 5.3dB, 6.5dB and 5.3dB, respectively

The power and gain will be sensitive to the relative values of the circuit elements, as these elements alter the loaded and unloaded Q of the device/circuit. This is illustrated in figure 27 for the case of the PBT structure A, a driving frequency of 40GHz and a natural circuit frequencies of 60GHz and 80GHz. In figure 27, the unloaded Q of the resonant circuit (see

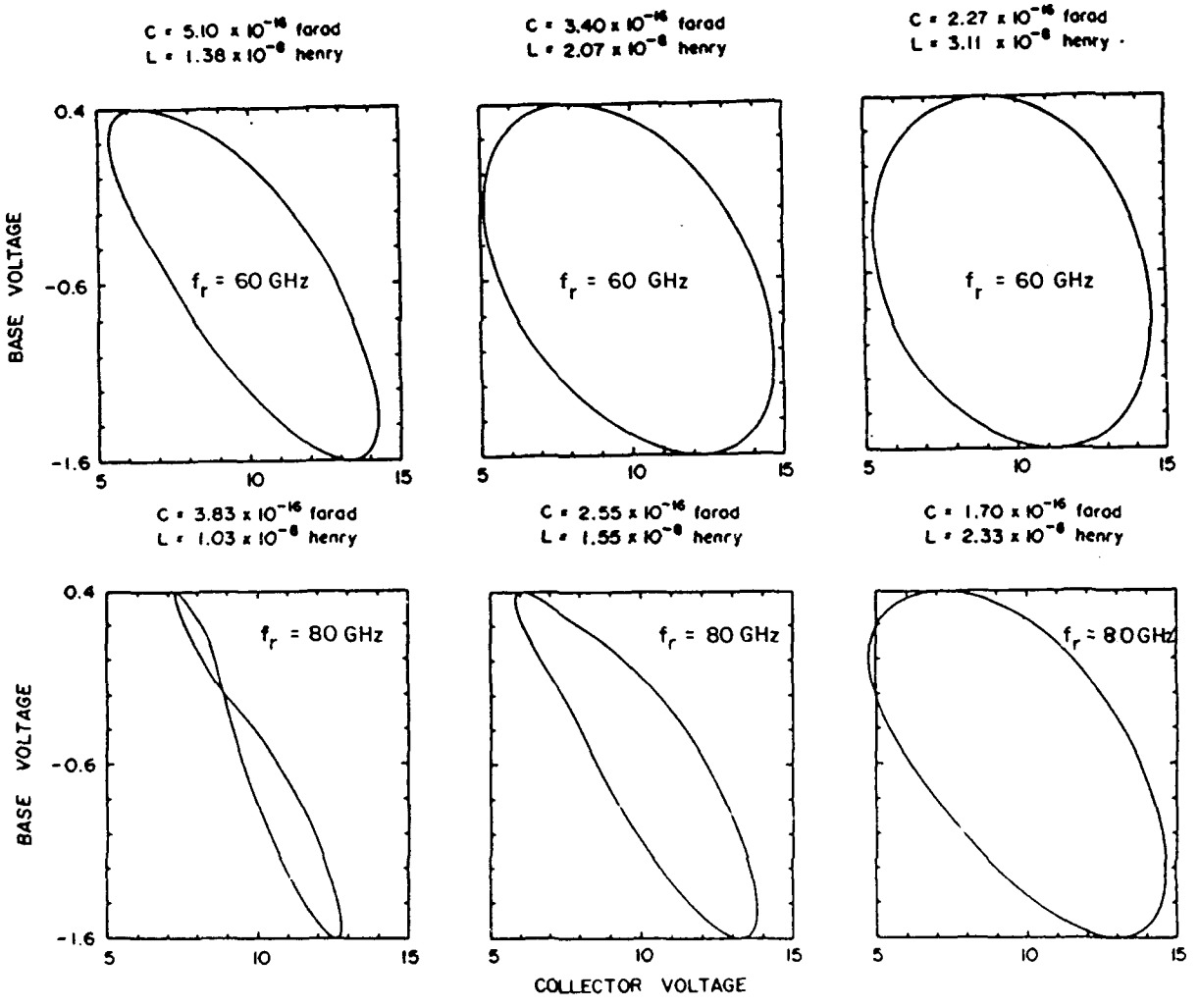


Figure 27. Base-collector lissajous for $V_b(0) = -0.6v$, $V_b = 1.0v$, $f = 40GHz$, $f_r = 60GHz$, and different values of capacitance and inductance.

equation 37) has successively lower values from left to right. The respective power gain for these decreasing Q circuits are respectively, 7.1dB, 6.2dB and 5.7dB for the resonant circuit with frequency 60 GHz; and 4.0dB, 6.7dB, and 7.0dB for the 80GHz resonant circuit. It is worthwhile noting that the unloaded resonant circuit Q for the 20GHz and 40GHz calculations of figure 26 are equal. This of course indicates that the loaded Q are to be included in all of the calculations.

Figure 28 displays the base current-voltage lissajous as well as the collector current-voltage characteristic. Of interest here is the collector characteristic in that it shows that there is a full lissajous, as opposed to the straight line displayed in figure 25.

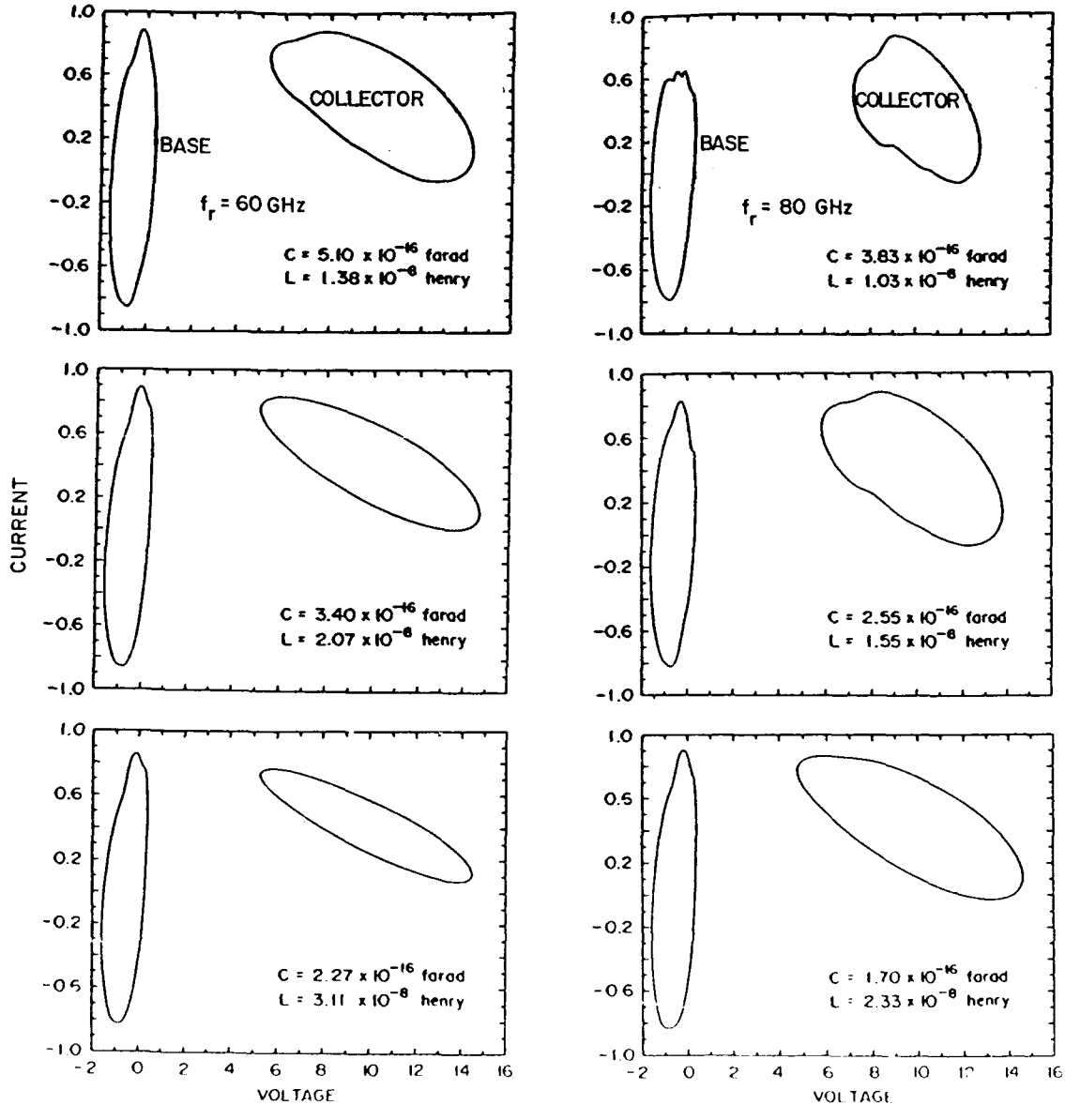


Figure 28. Base current-voltage lissajous and collector current-voltage lissajous for the parameters of figure 27.

What is the significance of the above calculations. In a recent study by Halkias, et al [2] the issue was raised as to whether it is possible to drive a unilateral amplifier above its classical class A value. Snider [3] demonstrated that under low frequency conditions it was possible to drive it at 1.62 times its classical value.

Halkias, et al [2] argue that to achieve high output values at high frequencies the assumption of a pure resistive load may not be the best choice. Even at X-band frequencies with small signal operation, they expect that the matching load impedances would yield a drain current -voltage lissajous (referred to as the dynamic diagram of operation in their study) which would be an ellipse (assuming no distortion). The major axis of this IV lissajous makes, under linear operation, an angle θ with the voltage axis, as displayed in figure 29, with θ depending on the real and imaginary parts of the load impedance.

As discussed by Halkias, et al [2], high frequency operation under standard small signal conditions does not lead to optimum output conditions. For example, as shown in figure 30 for a relatively small input power (1 mw), the ellipses, which correspond to the fundamental frequency are inclined with a small angle θ, small increases in power result in distortion of the lissajous with the result that clipping of the output signal occurs. At higher input levels the angle θ increases but as long as the dc point is close to the knee voltage significant distortion will occur, as shown in figure 31a. Moving the dc points further away from the knee voltage results in a more moderate value of θ, less distortion and the possibility of design for higher output.

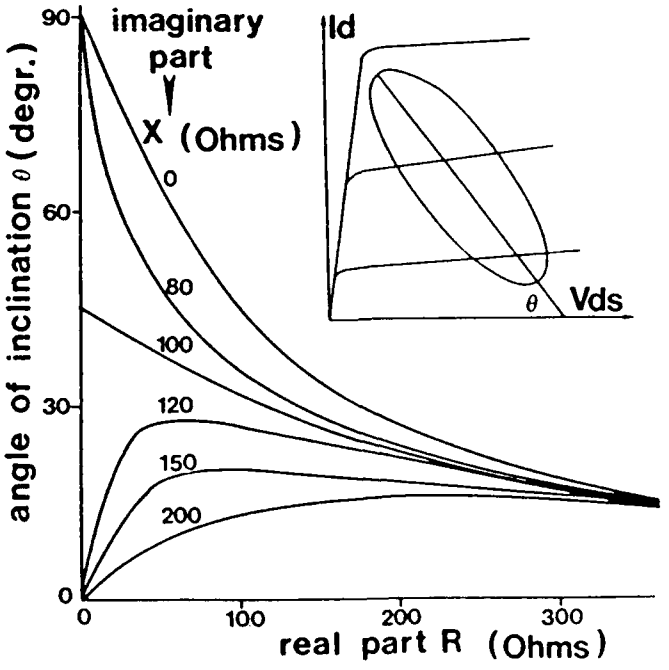


Figure 29. Angle θ between the major axis of the ellipse (corresponding to linear AC operation a three terminal structure) and the voltage axis of the static output characteristics as a function of the real part (R) and the imaginary part (X) of the load impedance (From ref (2)).

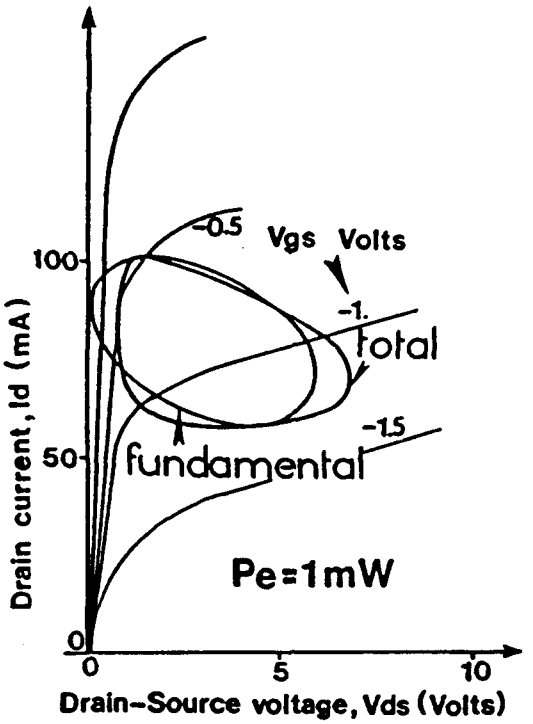


Figure 30. Drain current-voltage lissajous for an input power of 1 mw a source-drain voltage of 3v, and a gate source voltage of -0.9v (these values are from ref (2)).

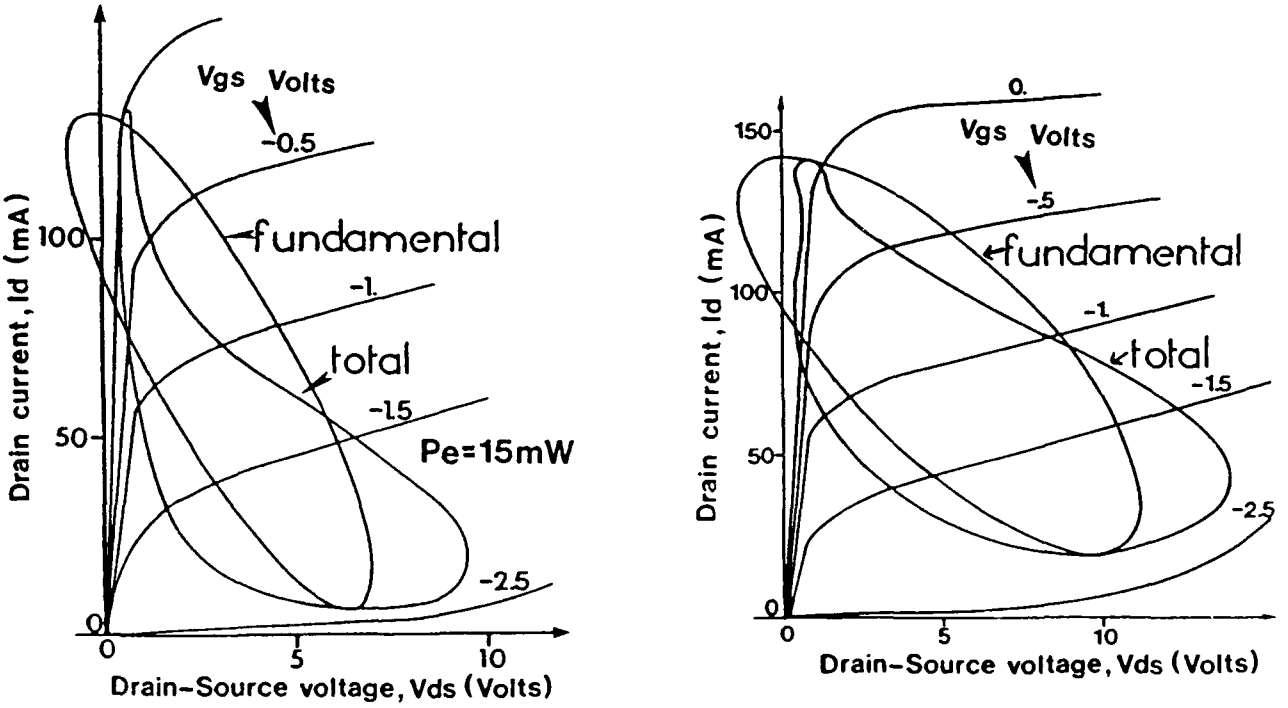


Figure 31. (a) Drain current-voltage lissajous for an input power of 15 mw a source-drain voltage of 3v, and a gate source voltage of -0.9v (these values are from ref (2)). (b) As in (a) but for a source-drain voltage of 5v.

In the calculations performed in this study that have been discussed above (see figures 18 through 28) the voltage swings do not go to the knee of the dc IV curves and the power calculations show linear behavior, at least for the range of bias considered. These results are shown in figure 32. The calculations for gain were performed for a single PBT. However the axes which indicate the input and output power are obtained for an array of 150 identical PBT cells and a depth of 25 microns. **The results suggest the remarkable result that for the repetitive structure considered that an output power of 70mw at 40 GHz is a distinct possibility.**

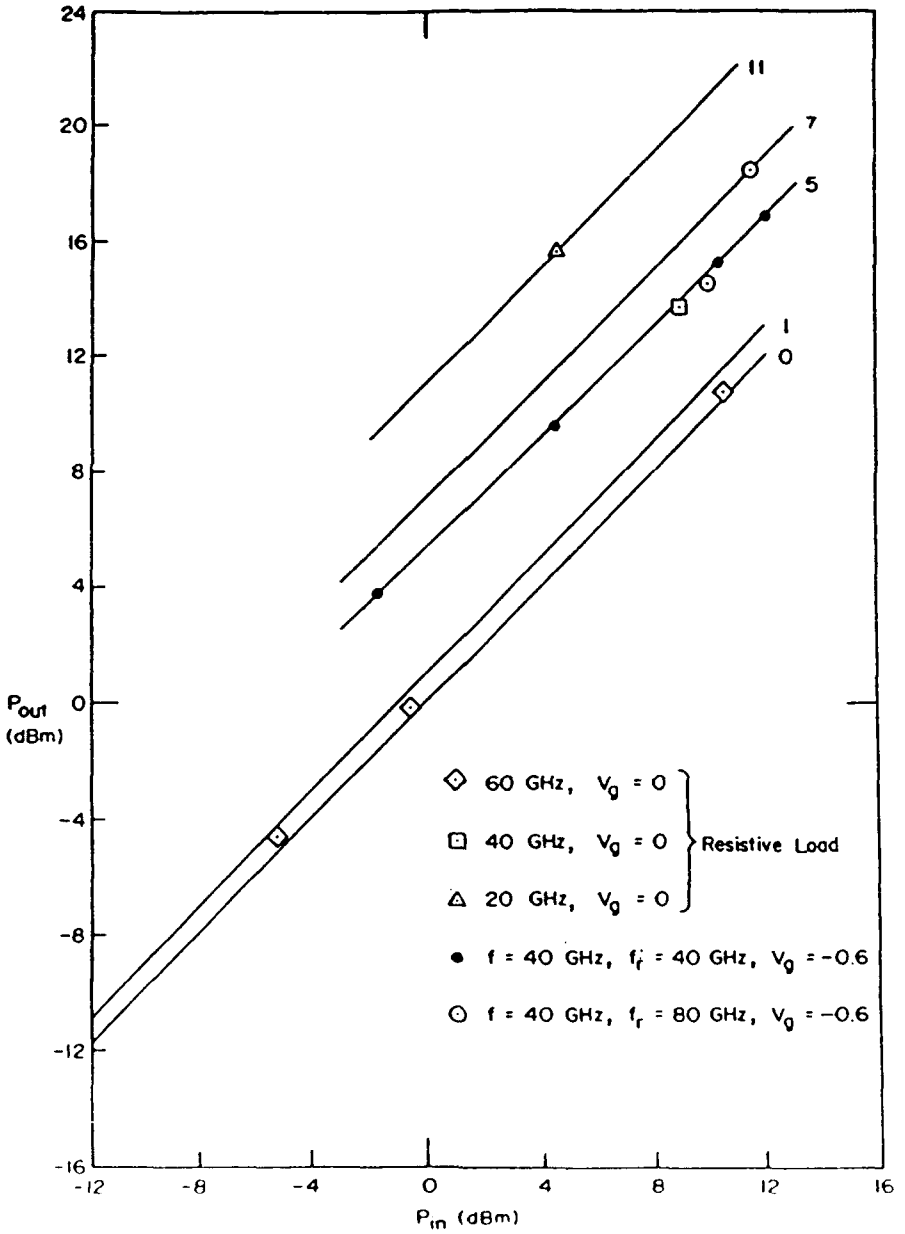


Figure 32. Power gain at select points for 150 identical PBT structures with a 25μm depth. Straight lines are drawn for reference.

LINCOLN LABORATORIES/SRA PBT DESIGN

The above results concerning the design of the structure as well as the large signal behavior were transmitted at various stages to workers at Lincoln Laboratories. A new structure was agreed upon and calculations were performed. The structure is shown in figure 33. Figure 34 displays the dc IV characteristics for this structure.

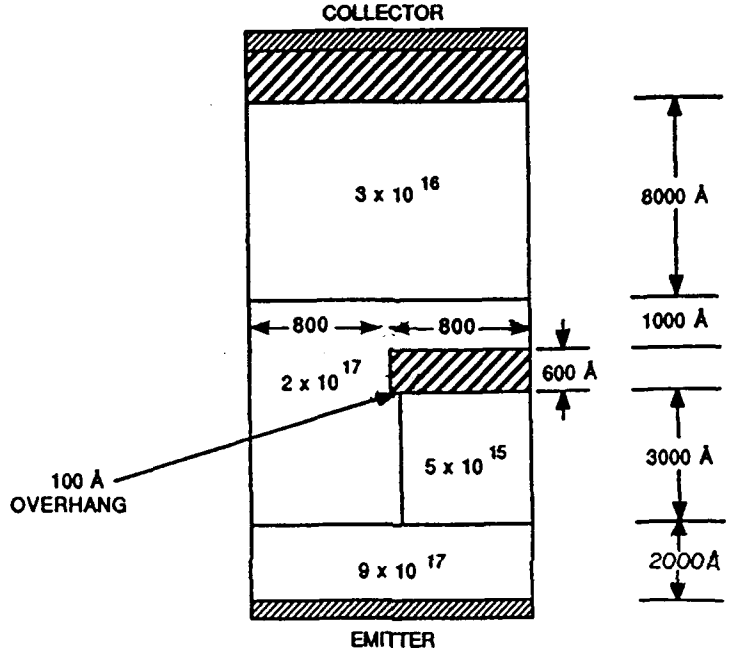


Figure 33. Lincoln Laboratories/SRA PBT design.

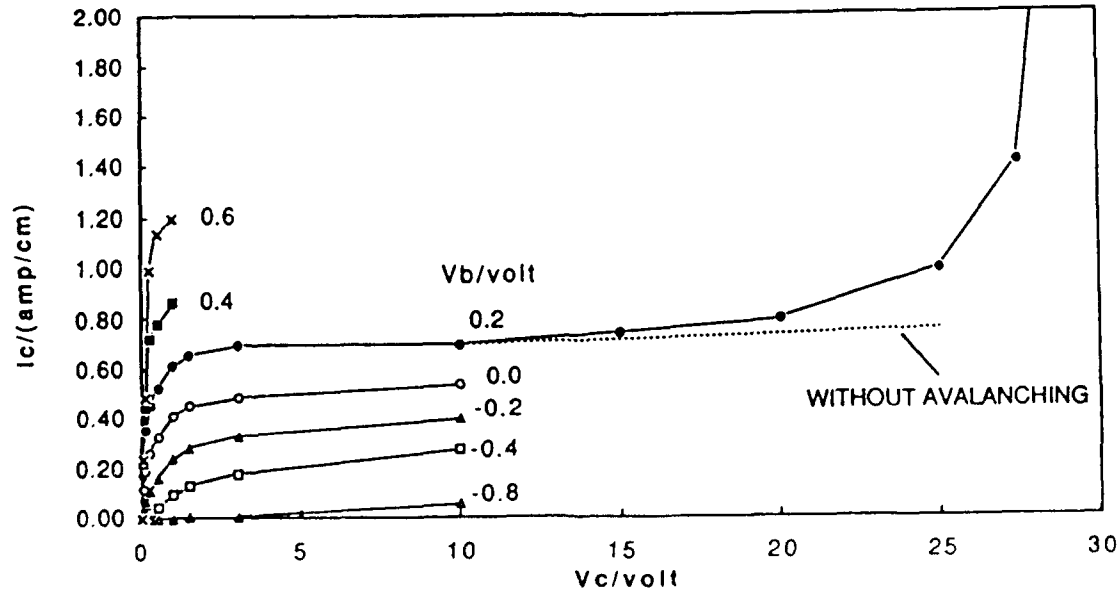


Figure 34. DC IV characteristics for the structure of figure 33.

There are a number of critical features that emerge from the DC characteristics. The first is that the breakdown occurs at voltage levels higher than that of any of the previous structures. We note that in the previous nonuniformly doped structures the largest breakdown occurred in that structure with the longest collector region. This tended to reduce the local field in the device relative to those structures with shorter collector regions. The new structure also exhibited a lower threshold voltage than that of the uniformly doped PBT. This would imply that voltage swings under AC operation may lead to larger distortion in the output of the new structure compared to that of the uniformly doped PBT. The threshold voltages are displayed in figure 35, where the square root of collector current is plotted as a function of base voltage. The cutoff frequency is higher than that of the uniformly doped PBT as displayed in figure 36, where it is emphasized that at a bias of 10v on the collector, the cutoff frequency is relatively insensitive to the base voltage.

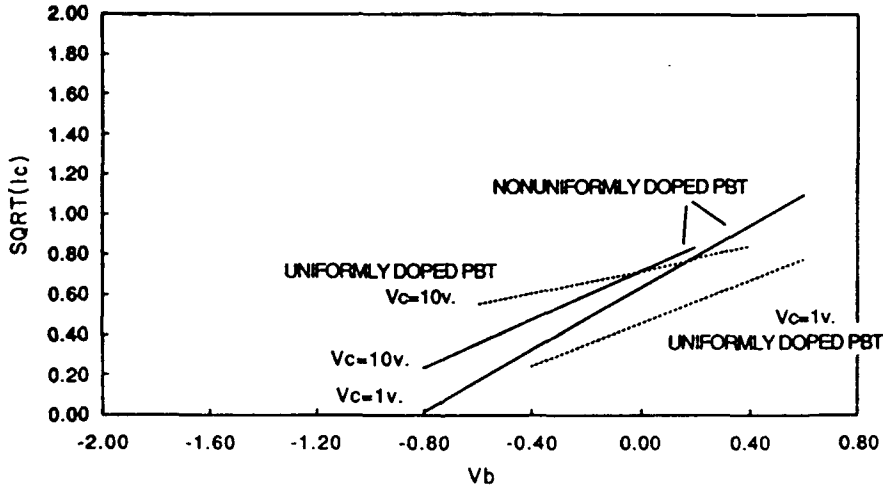


Figure 35. Square root of the collector current versus base voltage. An extrapolation to zero collector current yields the threshold voltage. From DC results.

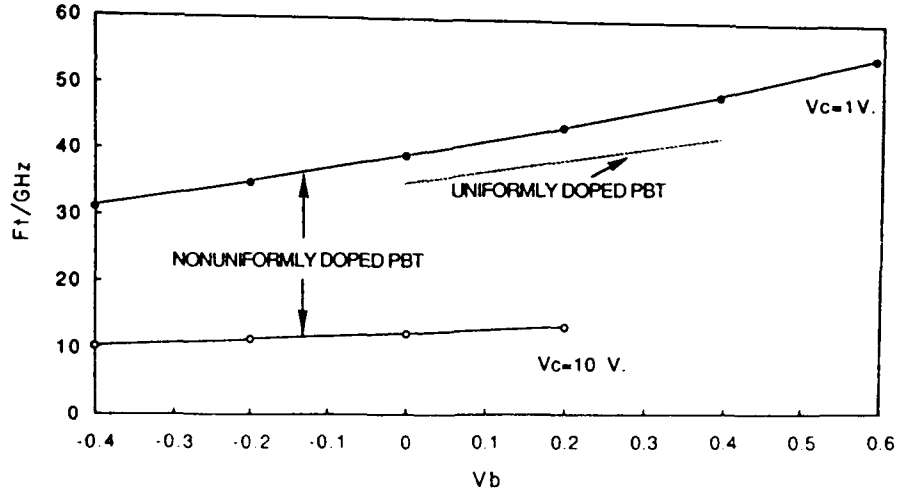


Figure 36. Cutoff frequency versus base voltage.

The calculations discussed above were taken from the dc calculations. Small signal time dependent calculations were also performed at select bias points to confirm some of the above conclusions. For example, figure 37 displays the maximum current gain as computed from the semiconductor drift and diffusion equations for the case of a small time dependent step change base and collector bias. The current gain as computed from equation 10 for a base voltage of 0.2v and a collector voltage of 1.0v is displayed in figure 37. The cutoff frequency is closer to 50GHz then the dc calculations indicate. In figure 38 we display the maximum available small signal gain for this structure as computed from equation (12). This yields an f_{max} of approximately 170 GHz. We note that the stability factor indicates values greater than unity for frequencies in excess of 90 GHz.

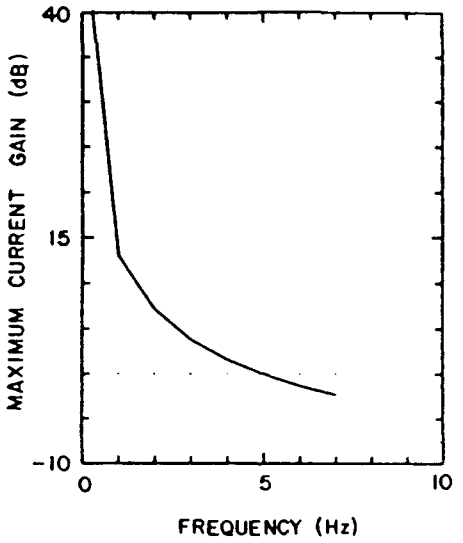


Figure 37. Maximum current gain as computed from equation (10) for $V_b = 0.2v$, $V_c = 1.0v$.

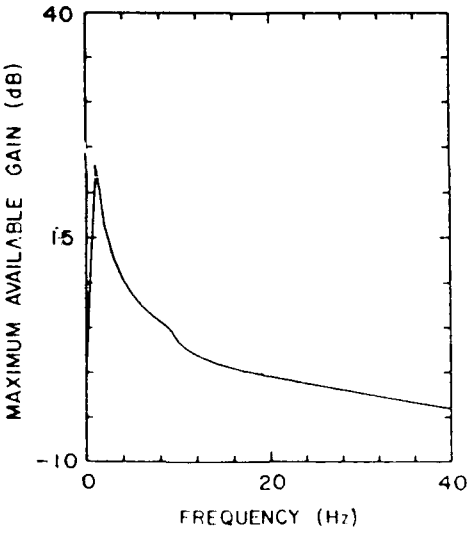


Figure 38. Maximum available gain as computed from equation (12) for $V_b = 0.2v$, $V_c = 1.0v$.

Large signal calculations with this structure were also performed. The dc points for this calculation were $V_b = -0.4v$, $V_c = 10.0v$. The amplitude of the base voltage varied from 0.2v to 1.0v. Thus the current swings on the collector and emitter were below zero. The base frequency was taken as 40GHz, as was the resonant circuit; thus the collector current-voltage lissajous was a straight line as in figure 25. The base-collector lissajous is shown in figure 39. The slope of the major axis shows a greater tilt in the first quadrant than that of the calculations of figure 21. We note that in this calculation we have not varied the circuit parameters (keeping the natural frequency fixed). Previous experience indicates that for a resonant frequency equal to the driving frequency, the power gain is unchanged.

The output power versus the input power for this structure is shown in figure 40. Note that the gain decreases with increasing input power. For comparison, a straight line is drawn against the curve asymptotically approaching the low input curve. The 1dB and 2 dB compression points are noted.

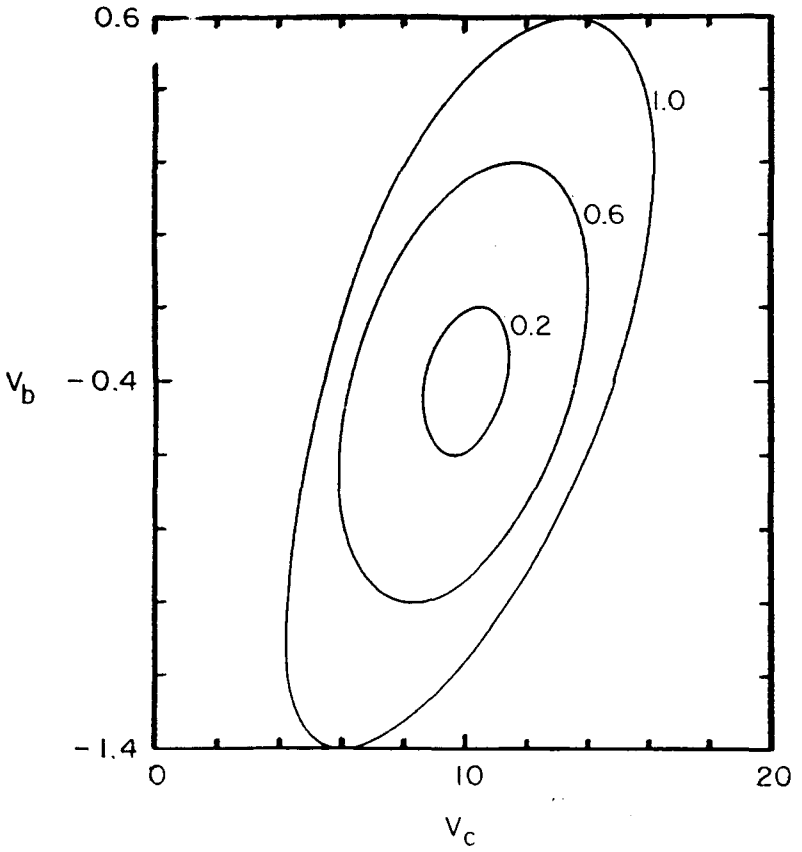


Figure 39. Gate-drain voltage lissajous for the structure of figure 33. For this calculation $V_b(0) = -0.4v$; $V_b = 0.2v, 0.6v, 1.0v$; $V_c = 10.0v$, $f_r = f = 40$ GHz.

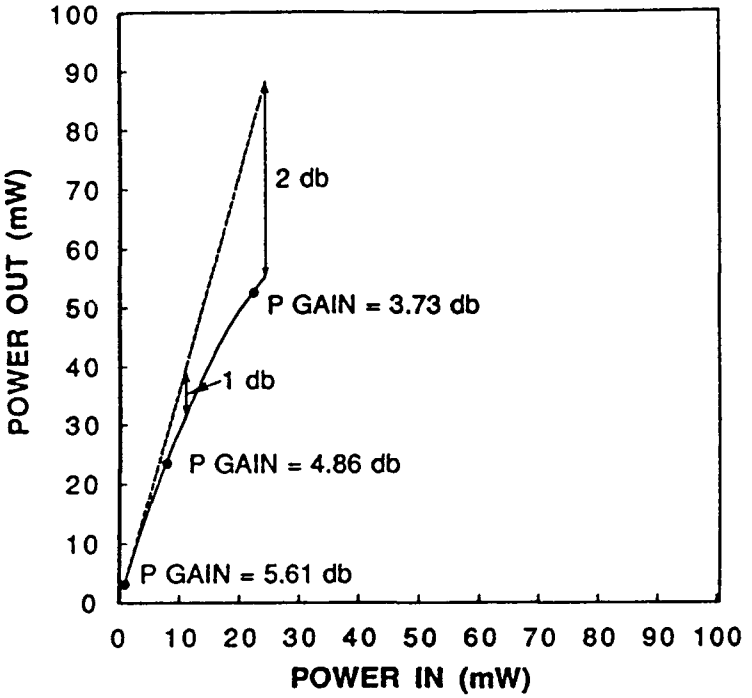


Figure 40. Output power versus input power for the structure of figure 33.

EXTENSION OF THE LARGE SIGNAL SIMULATIONS TO CAD PROGRAMS

One of the remarkable features of the above study, is that the approach taken at SRA was one not taken earlier by other workers in the EHF field. Most of the earlier studies involved approximating the dynamics of the operation of the device by analytical formulae, coupled to ordinary differential equations. The advantage of the ordinary differential approach to the study of devices is speed.

In the course of this study, SRA was awarded an NSF program to introduce an ordinary differential equation approach to examining high frequency devices based upon the DARPA program. Because of its relevance to future EHF studies and because it is a direct outgrowth of the DARPA program we summarize it below.

The calculations discussed above are designed to determine those conditions in which devices are most suitable for EHF applications. Once this is known, the next step is to transfer the output of the results in a form that will enable circuit and systems engineers to incorporate the chosen devices with their known electrical properties into complex circuit configuration for specific applications. It is these applications that are driving the device and circuit design.

The ideal way to transition the technology from the device physics, to the device-circuit

interaction, to the device-system interaction, is to deliver to the systems engineer a time dependent code that will incorporate all of the partial differential equations describing the device, and the ordinary differential equations describing the circuit. Now it is well known that performing calculations using the drift and diffusion equations or the moments of the Boltzmann transport equation is impractical for engineers who are designing circuits into which gallium arsenide devices are to be inserted. The reason is the long run times even with todays largest and most advanced supercomputers. Because such procedures are impractical, engineers have been using other means to design systems using complex nonlinear electronic devices.

One common approximate approach to allow practical device circuit interfacing is to obtain analytical approximations for the dc current voltage characteristics of a given three terminal device, as well as analytical approximations for the relevant capacitances of the device, and then lump these parameters into a large signal simulator that solves the following set of coupled ordinary differential equations:

$$(39) \qquad I_d(t) = I_{d_o}[V_d(t-t_o), V_d(t)] + C_{gd}[dV_g/dt] + C_{dd}[dV_d/dt$$

$$(40) \qquad I_g(t) = I_{g_o}[V_g(t), V_d(t-t_1)] + C_{gg}[dV_g(t-t_2)/dt] + C_{dg}dV_d(t)/dt$$

In the above the terms t_0, t_1, t_2, represent time delays associate with transit of carriers between the gate and drain, drain and gate, and source and gate, respectively. The capacitive contributions are functions of the gate and drain voltage, with the time delays appropriate to the equation in which they appear.

Equations of the type represented by equations (39) and (40) have been coupled to harmonic balance programs, with the small signal parameters are "SPICE"-like compound semiconductor circuit representations and used to obtain the admittance and scattering matrices needed to evaluate the small signal properties of three terminal devices.

Recently SRA, under NSF sponsorship, has approached the generation of the coefficients of the circuit equations (39) and (40) from a general point of view. Rather than use analytical procedures for obtaining these coefficients, they are obtained from the governing device equations. The procedure for accomplishing involves six broad steps. These are identified below in terms of solutions to the drift and diffusion equations, although the procedure is equally valid using the moments of the Boltzmann transport equation:

(1) From the dc characteristics of the device, as obtained from the DDE the bias dependent dc drain and gate currents are obtained, as is

(2) the net change in charge on the drain and gate contacts for a change in voltage on the gate contact. This latter procedure leads to C_{gg} and C_{gd}.

(3) A similar procedure leads to a calculation of C_{gd} and C_{dd}.

The transient results suggest that there will be a transit time delay associated with the imposition of a signal on the gate contact and its observation on the drain contact. Similarly a change in voltage on the drain contact will have its effect on the gate contact delayed.

(4) The time delays associated with this are represented by the terms t_0 and t_1.

(5) There is also a time delay associated with the source-gate loop, and this is represented as t_2.

Transient calculations performed with the DDE at select bias points and calculations performed with the ODE representation of the device demonstrate that the transient behavior of the device can be well represented by a nonlinear lumped circuit element, at frequencies for which the procedures were tested, namely from 20 to 60 GHz. This is illustrated below. The use of the ODE representation of device, based upon the physical DDE and MBTE models indicates that important design procedures associated with varying the doping profile of the structure, the size of the structure, the placement of the contacts can be incorporated realistically into advanced circuit simulators. Further once the advanced circuit simulators are used as tool for designing a device circuit system,

(6) Select calculations using the full drift and diffusion equation algorithm can be invoked at select bias points to verify and they modify, as needed, the circuit design structure.

We illustrate the above procedure next. Figure 41 is a sketch of a GaAs structure being for the above procedures were implemented. This structure was taken from the literature

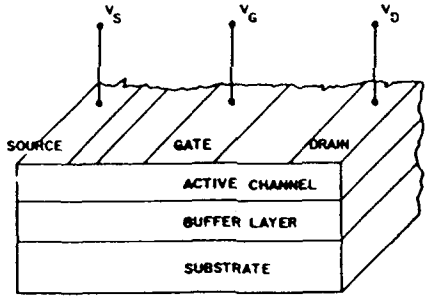


TABLE 1

PHYSICAL PARAMETERS FOR THE 0.5 μm GATE LENGTH GaAs MESFET USED IN THE SIMULATION

GATE LENGTH	0.55 μm
GATE WIDTH	300 μm
CHANNEL THICKNESS	0.15 μm
SOURCE TO GATE SPACING	0.5 μm
DRAIN TO GATE SPACING	0.6 μm
BUFFER LAYER THICKNESS	0.2 μm
GATE METALLIZATION	ALUMINUM
SCHOTTKY BARRIER HEIGHT	0.80 V
TEMPERATURE	350 K
DOPING OF ACTIVE LAYER	1.5×10^{23} m^{-3}
DOPING AT CONTACTS	3.7×10^{23} m^{-3}
SUBSTRATE IMPURITY LEVEL	1.0×10^{23} m^{-3}

Figure 41. Structure and physical parameters of the GaAs MESFET taken from ref. (4).

[4], and used because data exists. Figure 42 is a sketch of the dc IV curves obtained by solving the semiconductor drift and diffusion equations. The calculations performed at SRA included avalanching. For comparison in the calculation we also show experimental results for this structure as well as calculations performed by Snowdon et al [4]. Measurements beyond 5 volts were not available; and the SRA calculations show breakdown at 5 volts. Note that at -1.0v and -2.0v on the gate the agreement between the SRA calculation and measurement is excellent. Deviations at low gate bias levels are likely due to the presence of avalanching. At the high bias levels the deviations are most likely due to heating, which causes a lowering of the mobility.

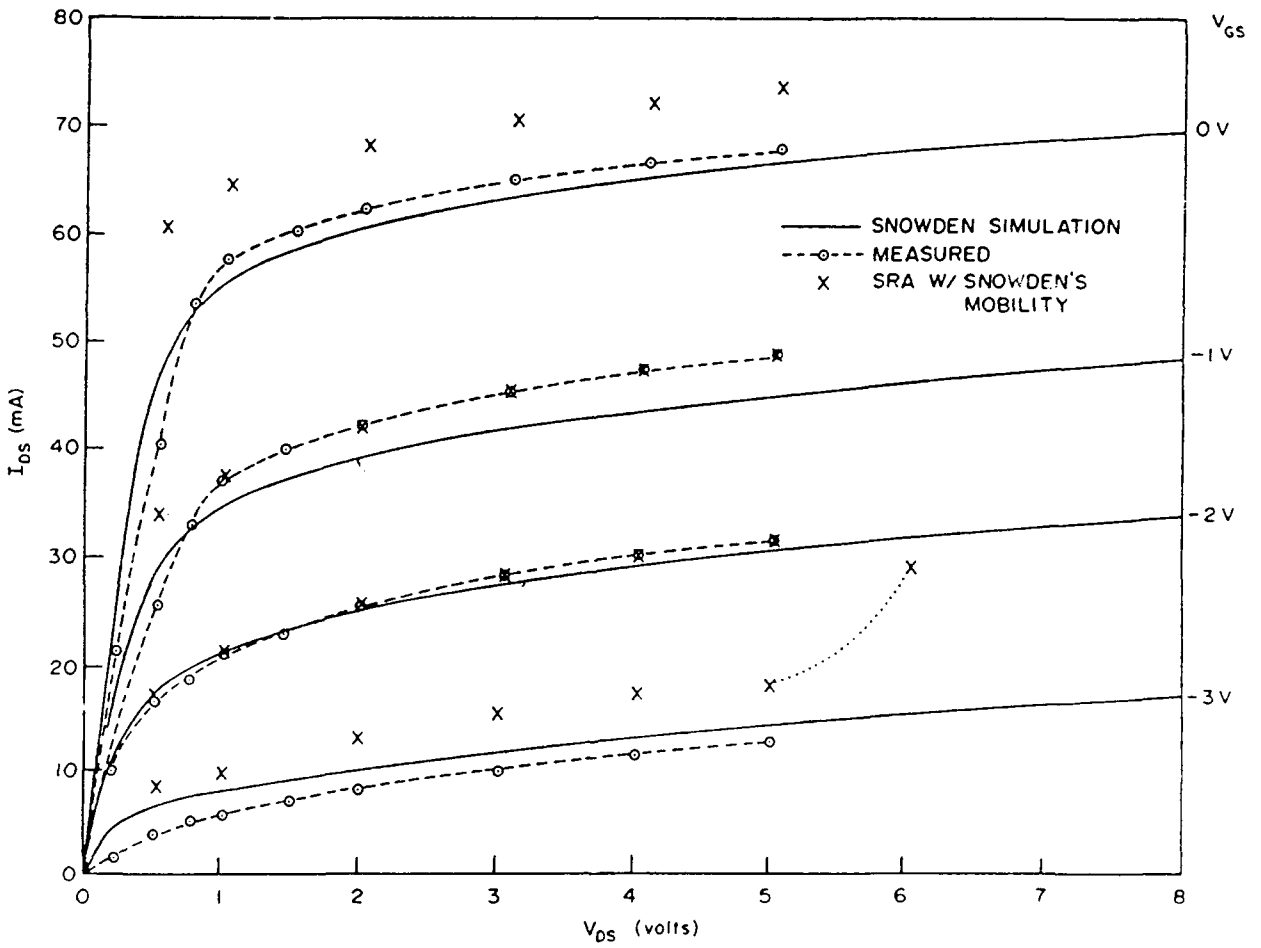


Figure 42. DC IV characteristics of the structure of figure 41.

Transient calculations were performed with the gate driven by a rf signal and the drain connected to a resistive load. These calculations were performed for both the drift and diffusion equations (14) through (20), and the circuit equation (39) and (40). Figure 43 displays the gate and drain voltage versus time for this calculation. The imposed gate voltage is the same for both the DDE solver and the ODE solver. The drain voltage calculation is performed self-consistently for both the DDE and ODE description and is also displayed in figure 12 for a 20 GHz driving signal. Apart from variations at the early part of the transient the ODE and DDE solutions are remarkably similar. For these calculations there is an apparent phase difference between the gate and drain voltages. The origin of this phase difference is direct. Under dc conditions an increase in gate voltage is accompanied by an increase in drain current. For the drain being connected to a resistive loop, an increase in drain current results in a decrease in drain voltage. Thus in the absence of any time delays associated with carrier transport, a minimum in gate voltage should be accompanied by a maximum in drain voltage. The details of the calculation show that the minima in gate voltage and the maxima in drain voltage are shifted by a finite amount. This phase relationship is summarized in figure 44, which is the lissajous for both the DDE and ODE solvers. Figure 45 displays the gate current calculation for both the ODE and DDE calculations; again the agreement is excellent. Now ideally if the gate capacitor were not voltage dependent the gate current would be $\pi/2$ out of phase with the gate current, and a plot of the lissajous of gate current and gate voltage would be an ellipse (or circle, depending on the normalization). Transit time delays affect this phase relation, as the lissajous of gate current and gate voltage, shown in figure 46 illustrates. The drain lissajous is a straight line, reflecting the resistive load in the drain loop.

At high frequencies the results are different. Here it may be expected that the for sufficiently short oscillation periods the movement of the depletion layer is negligible in response to changes in the gate bias. For this case increase in gate bias are accompanied by current transients from the source to the gate, and locally from regions of the drain side of the gate depletion region to gate contact. The result is a net decrease in drain current in response to an increase in gate bias. Since the drain voltage increases with decreasing current, the gate voltage versus drain voltage lissajous should shift and the two should move into approximate phase with each other. This is seen in figure 47. As discussed in the appendix, this phase relationship can be altered by means of an external circuit.

The only advantage of the ODE solver over that which incorporates solutions to the partial differential equations is **time**. If a system of ODE solvers can be used to replicate the output of the PDE then the ODEs can be effectively used by circuit engineers to represent the device in circuit codes. Now it is clear that obtaining an ODE solve to replicate the behavior of a device at one frequency is not a demonstration of its ability to perform this type of calculation at other frequency values or at other bias values. The results of the frequency dependence is demonstrated by a calculation of the product of power gain and versus driving frequency, for both the PDE and ODE solvers (see figure 48) apparent linearity suggest predictions at other frequencies. There is remarkable agreement between the two. Preliminary results with the bias dependence shows equally satisfactory agreement.

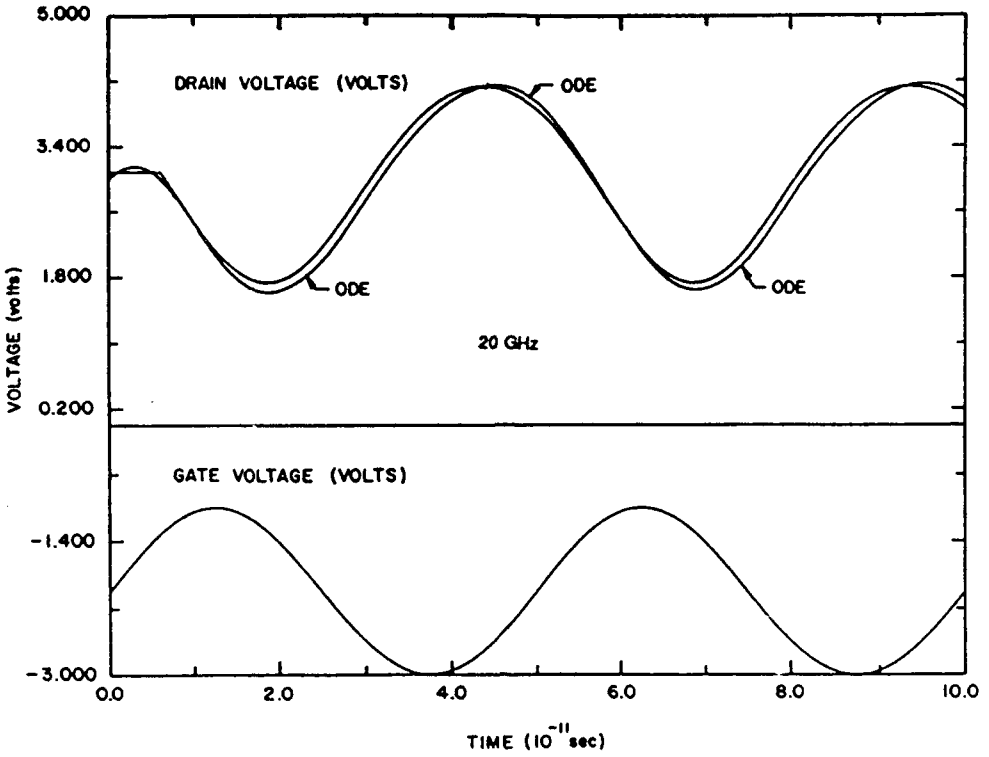


Figure 43. Time dependent drain and gate voltage for the ODE and DDE solvers. $V_g = -2+\sin(2\pi ft)$ V_d is nominally 3.0 volts.

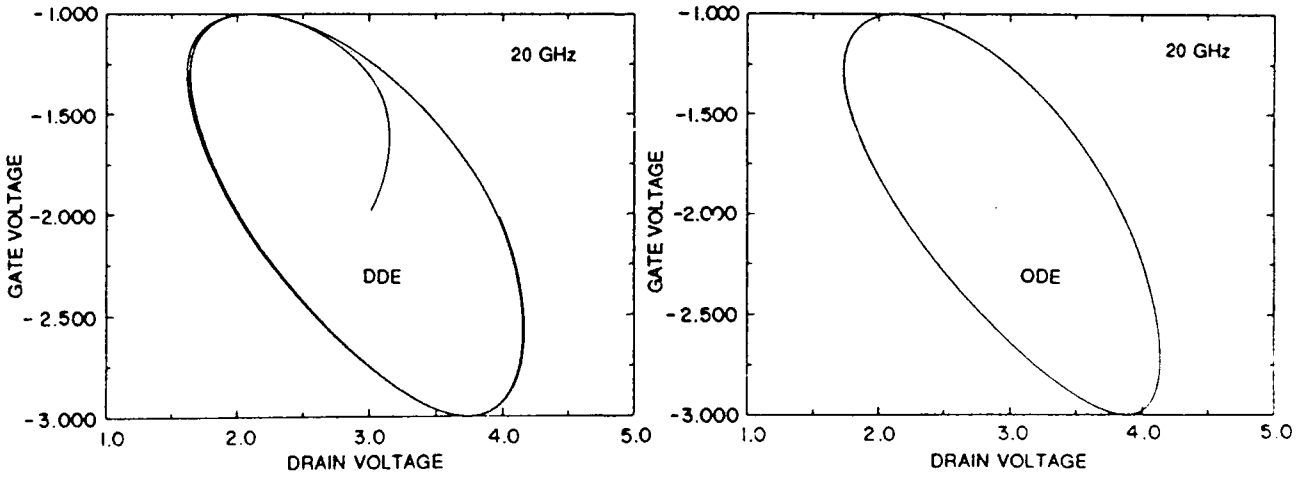


Figure 44. Gate and drain lissajous for the calculations of figure 43.

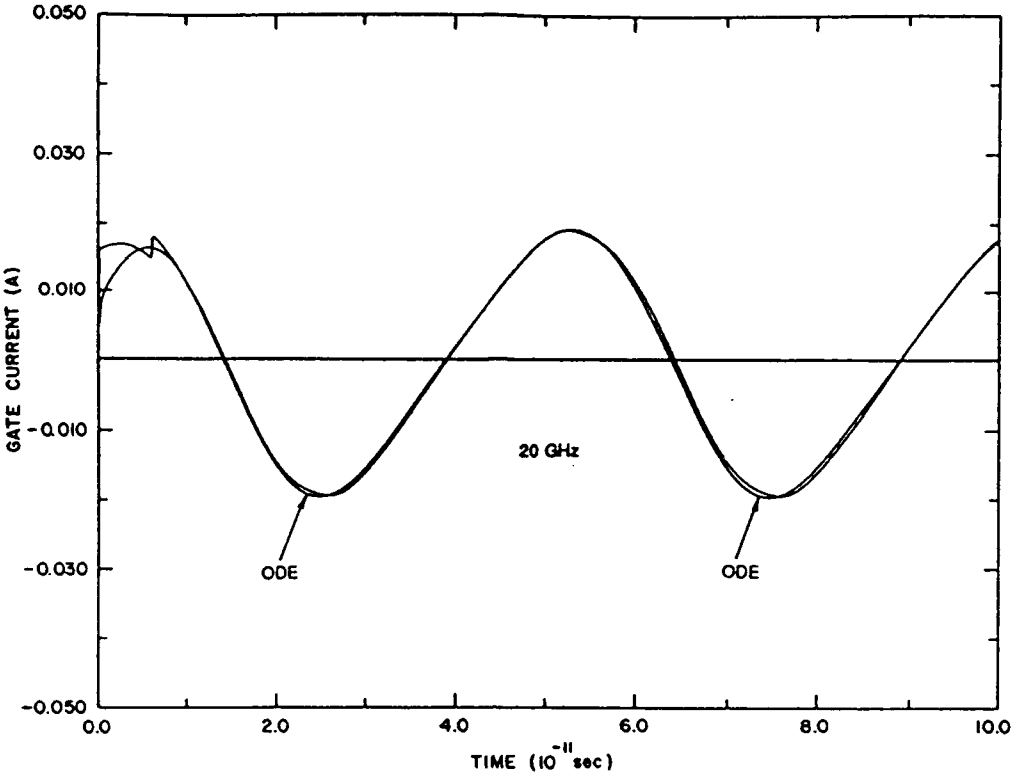


Figure 45. Time dependent gate current for the calculations of figure 43.

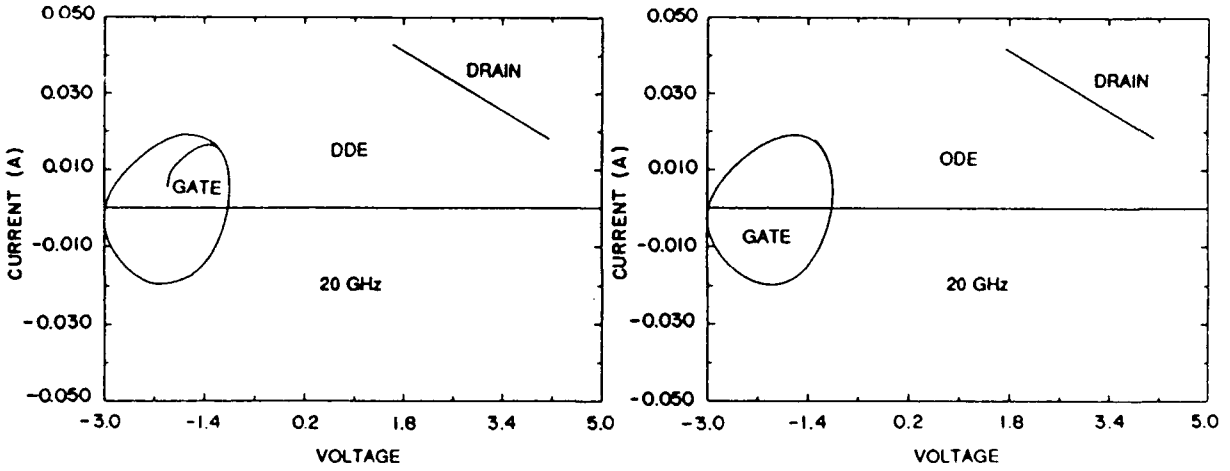


Figure 46. Gate current vs. voltage lissajous for the calculations of figure 43.

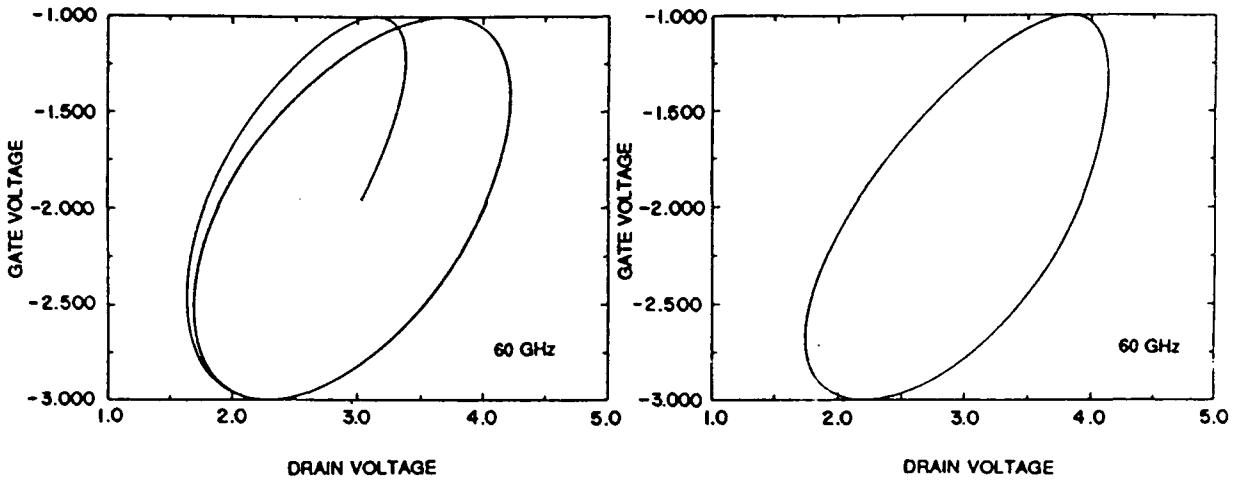


Figure 47. Time dependent gate current for the calculations of figure 43 with the frequency of the gate increased to 60 GHz.

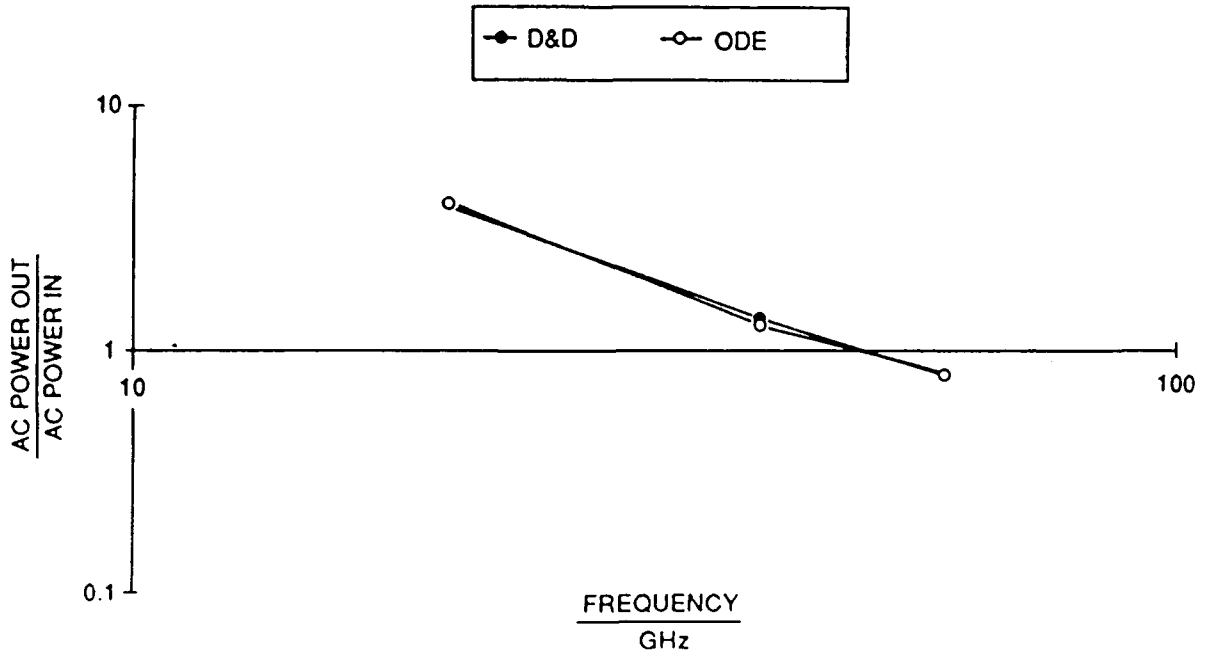


Figure 48. Power gain vs. frequency for the structure of figure 41 and $V_g = -2 + \sin(2\pi ft)$.

IV 2. OGST Calculations

The opposed gate-source transistor (OGST) was originally proposed by Dalman and Lee [5]. A schematic of a single OGST device is shown in Fig. 49. The device is symmetric about the centerline normal to the source and gate surfaces. The structure of the device is such that a doubling of the transconductance should be realized without an increase in parasitic capacitances. This should allow for higher frequency operation. A more significant result of this novel structure is that it allows for a distributed interaction [5,6], and initial estimates of the device performance indicated a cutoff frequency in the range of 106 GHz.

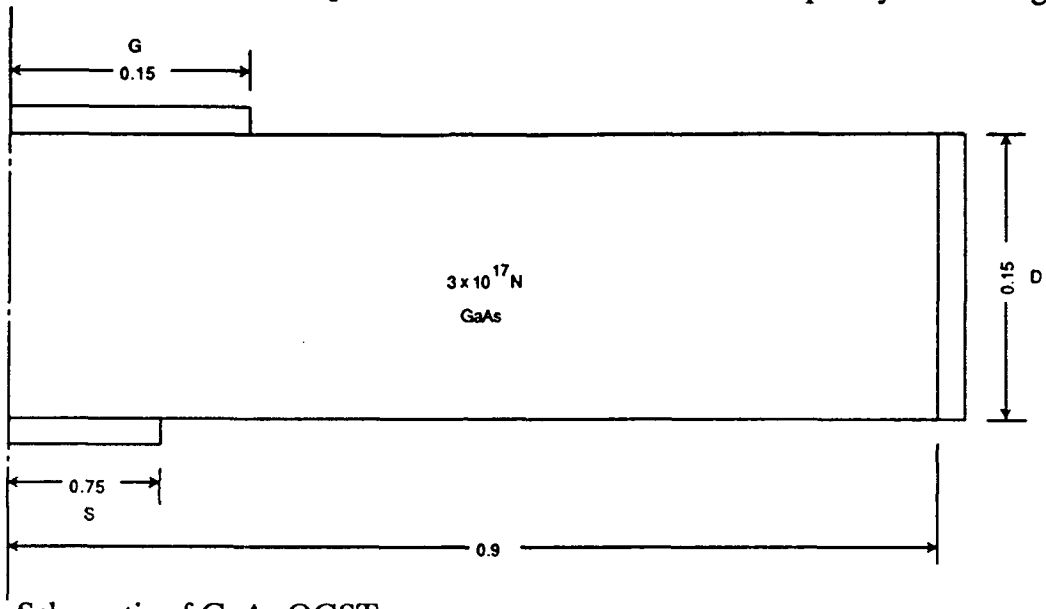


Figure 49. Schematic of GaAs OGST.

The GaAs OGST has been previously analyzed through numerical simulation by Krusius and Berenz [7]. In their approach they considered high field transport only within the formalism of the drift and diffusion approach. However, they examined two limiting cases. First, they considered the usual quasi-static approach in which the electrons are assumed to be in equilibrium with the local electric field. The short comings of this approach, applied to devices with small active regions and rapidly varying fields are well known. However, by proper choice of mobility and diffusion coefficients, hot electron effects and negative conductance may be considered. Never-the-less, the errors associated with the assumption of local equilibrium are ever present. Their second approach was referred to as a "ballistic" model. In this model, electrons are confined to the Γ valley conduction band and reduced carrier scattering is assumed in the device active region. As Krusius and Berenz point out [7], this is reasonable only if the electron energy does not exceed about 0.3 eV (the energy separation between the conduction bands in GaAs).

In the present study, two approaches are again taken. The first is similar to Krusius and Berenz's quasi-static approach in that the drift and diffusion equations are solved numerical with the inclusion of negative differential mobility. As will be discussed, the computed results show dramatically the shortcoming of this approach. In fact, at certain bias conditions it was possible to obtain non-unique solutions to this system of equations for the

OGST structure. The second approach followed here is much more general and physically realistic. Here we solve the moments of the Boltzmann transport equation (MBTE). Two level transport is considered (Γ and L valley), thus hot electron effects and nonequilibrium transport are accounted for. In addition, transient switching calculation are also performed.

The OGST structure considered is shown in Fig. 49. Here only one half of the device is shown. The entire device is symmetric about the centerline though the source and gate contacts. Thus, the device is 1.8μm between the left and right drain contacts, and 0.15μm wide (from the source to the gate). The source contact is 0.15μm long and the opposed gate 0.3μm long. The device considered is uniformly doped to $3x10^{17}$.

The current voltage characteristics, as computed from the DD simulations are shown in Fig. 50. Here we observe an interesting result. For V_{gs} = -1.6 and -0.8 volts, the I-V

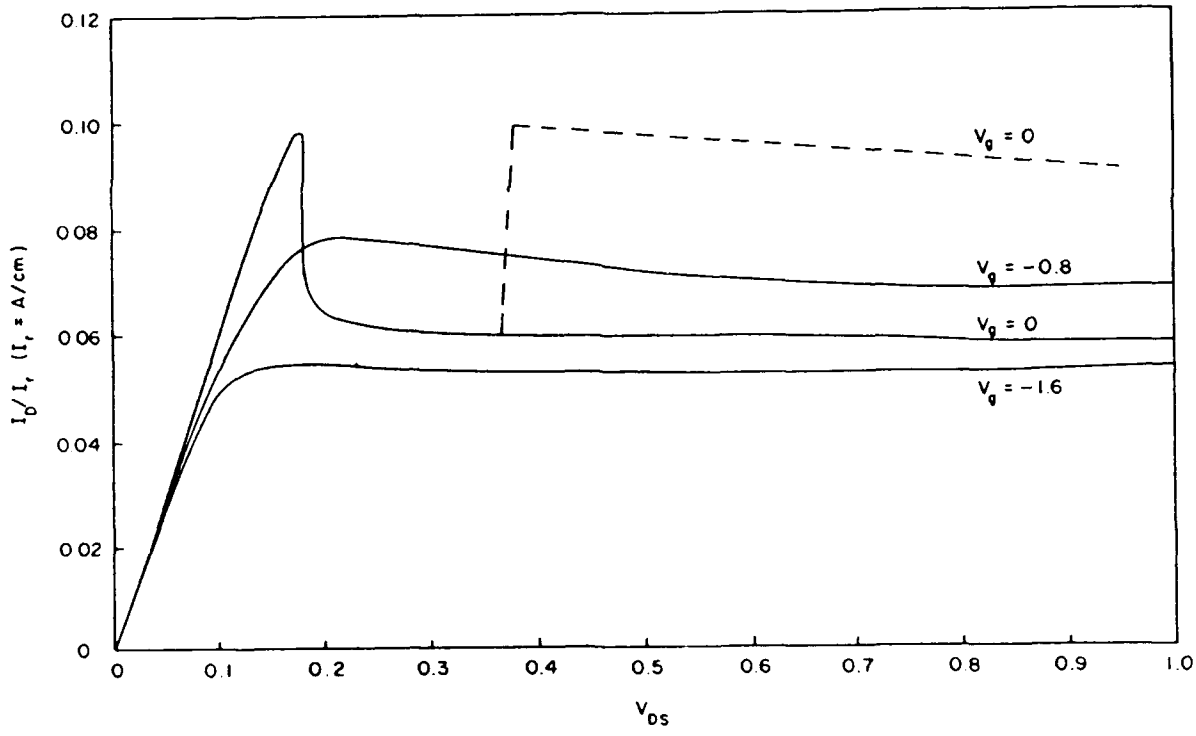


Figure 50. Current vs. drain voltage for OGST from drift-diffusion simulations. Broken line represents solutions where drain field is below the critical field (see text).

characteristics of the device are as would be expected, with the observation of a small negative conductance. However, for the case where $V_{gs} = 0$ an unusual result is observed. The current rises as the drain bias is increased, as expected, but after approaching what would be the knee of the curve, a precipitous drop in the current occurs. The current, for $V_{gs} = 0$ and V_{ds} greater than 0.18 volts drops below the current level for $V_{gs} = 0.8$ volts. These results are academically interesting since they serve to show the limitations of equilibrium assumptions inherent in the DD approach. The results is explained as follows: The DD simulations make use of a velocity-field relationship which includes a region of negative differential mobility with a peak velocity at what shall be referred to as the critical field, E_c. Above E_c the velocity decreases asymptotically to its saturated drift value. With this in mind, we examine the comparison of the carrier density and potential surface plots shown in Figs. 51 and 52. For the high current result at $V_{ds} = 0.18$ volts we see that the carrier density is uniform in the region of the source contact where as in the $V_{ds} = 0.185$ volts case there is a depletion region around the source contact. This results in the different potential distribution shown in Fig. 52. The differences in the distribution of potential in the proximity of the source contact are obvious. What is not obvious from this figure is the magnitude of the field in the region of the drain (the long flat region of the potential surface). In the high current case this field is very close to, but below the critical field, thus the carrier velocity is near the peak velocity. In the low current case the field in this region is above E_c and the velocity is reduced, giving a lower current.

For values of V_{ds} above 0.375 volts it was possible to generate stable solutions with higher current levels. This result is shown by the broken line in Fig. 50. These solutions required careful selection of the initial conditions and while they were stable, in that the drain bias could be swept between 0.375 and 1.0 volts without a switch to the low current solution, they could not be reached if started from a drain bias below 0.375 volts. Additionally, starting

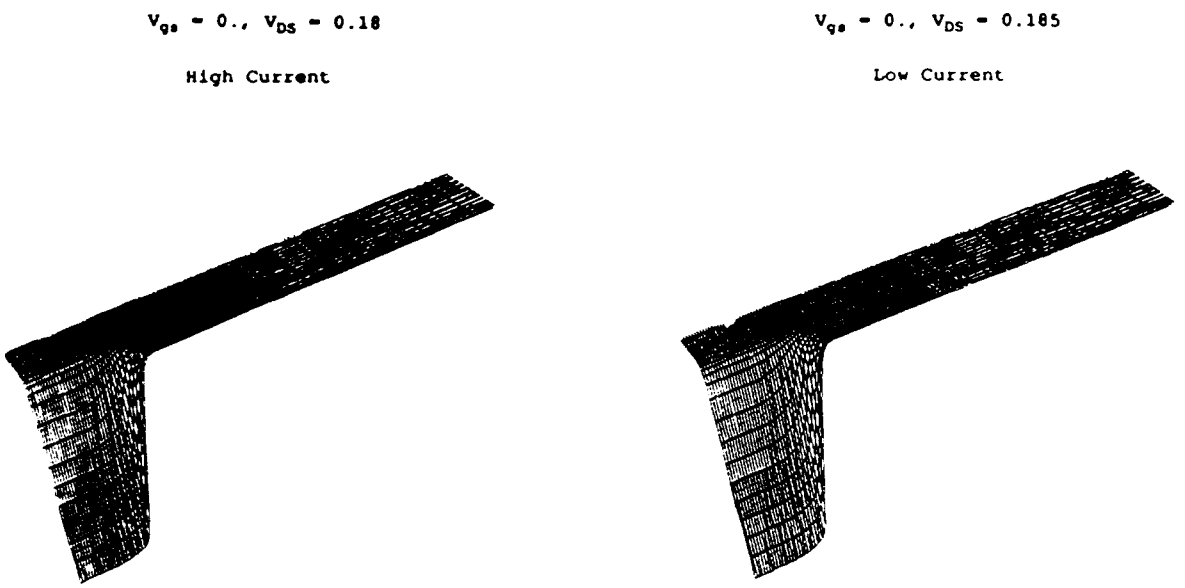


Figure 51. Comparison of carrier density distributions in OGST at $V_{ds} = 0.18$ volts (high current) and $V_{ds} = 0.185$ volts (low current) from drift diffusion simulation.

from the high current solution and reducing the drain bias below 0.375 volts resulted in having the solutions go to the low current result. Once on the low current curve, a jump to the high current result would not occur.

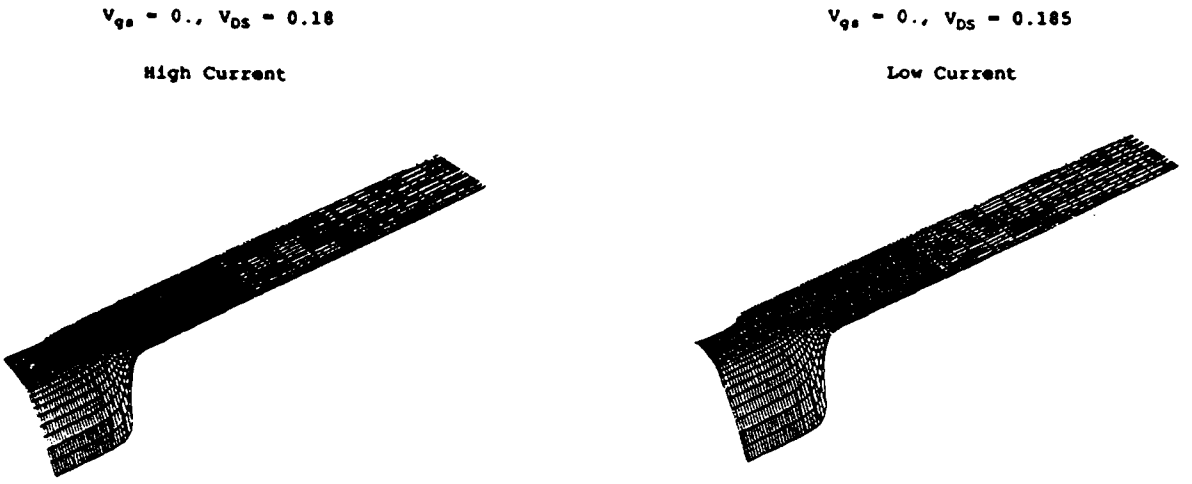


Figure 52. Comparison of potential distributions in OGST at V_{ds} = 0.18 volts (high current) and V_{ds} = 0.185 volts (low current) from drift diffusion simulations.

A comparison of the results for the high and low current solutions at V_{ds} = 0.5 volts is shown in Figs. 53 and 54. These results show more dramatically the difference in the solution characteristics. Fig. 53 shows the carrier density distributions. Again we see the depletion around the source contact in the low current case. In the high current case we notice a small ripple in the density emanating from the drain end of the gate depletion region. The potential surfaces, shown in Fig. 54, clearly indicate the different characteristics of the two solutions. In the low current case the field at the source contact is well above the critical field and the drift velocity well below the peak velocity. Carriers enter the device by drift, augmented by diffusion. In the high current case the electrons enter the device by drift only with the velocity very near the peak drift velocity. Again, while not apparent in the figure, the field in the drain region of the device is below the critical field in the high current case and above the critical field in the low current case.

As previously stated these results are of academic interest and serve to show the caution which must be exercised when using the DD approach in situations where the assumption of an equilibrium velocity field curve is questionable. To reveal the correct characteristic of the device a non-equilibrium transport model must be implemented. In the present study the MBTE approach was utilized. Fig. 55 shows the I-V characteristics of the device as computed from the MBTE simulations. Here we note that the predicted current levels are

significantly higher at saturation, as is typical of MBTE simulations compared to DD results.

Fig. 56 shows the distribution of the total carrier density and potential as computed for the OGST at $V_{ds} = 0.5$ volts and $V_{gs} = 0$ volts from the MBTE code. Here we note that the distributions exhibit characteristics of both the high and low current result from the DD simulation. Examining the carrier density, and referring to Fig. 53 for the DD result, we see that the variation of the carrier density normal to the source contact is similar to that of the high current DD result; no depletion is formed. However, just to the drain side of the source a depletion of carriers similar to the seen in the low current DD result is observed.

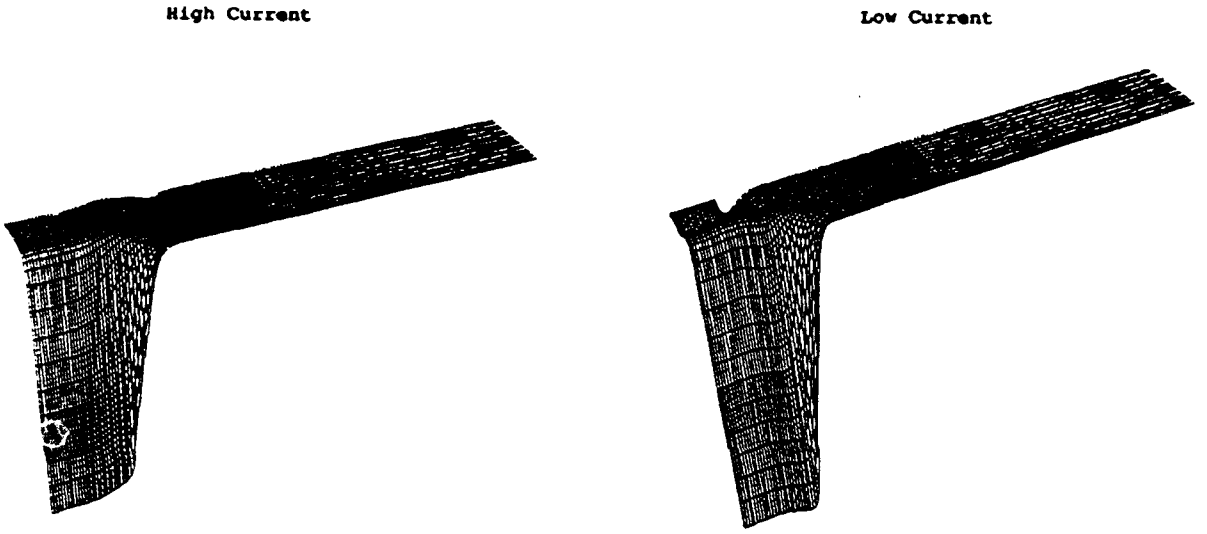


Figure 53. Comparison of carrier density distributions in OGST at $V_{ds} = 0.5$ volts and $V_{gs} = 0$ volts for high and low current branches of I-V curve.

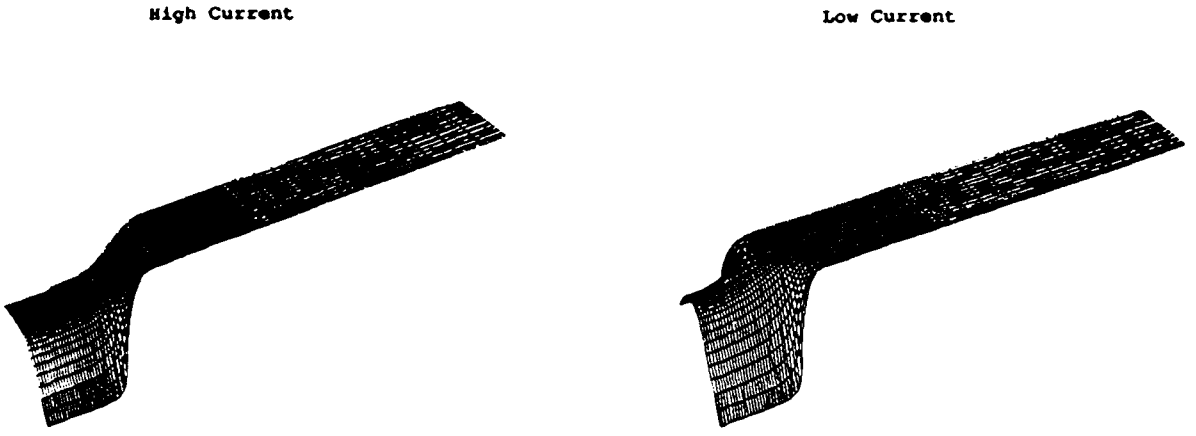


Figure 54. Comparison of potential distributions in OGST at $V_{ds} = 0.5$ volts and $V_{gs} = 0$ volts for high and low current branches of I-V curve.

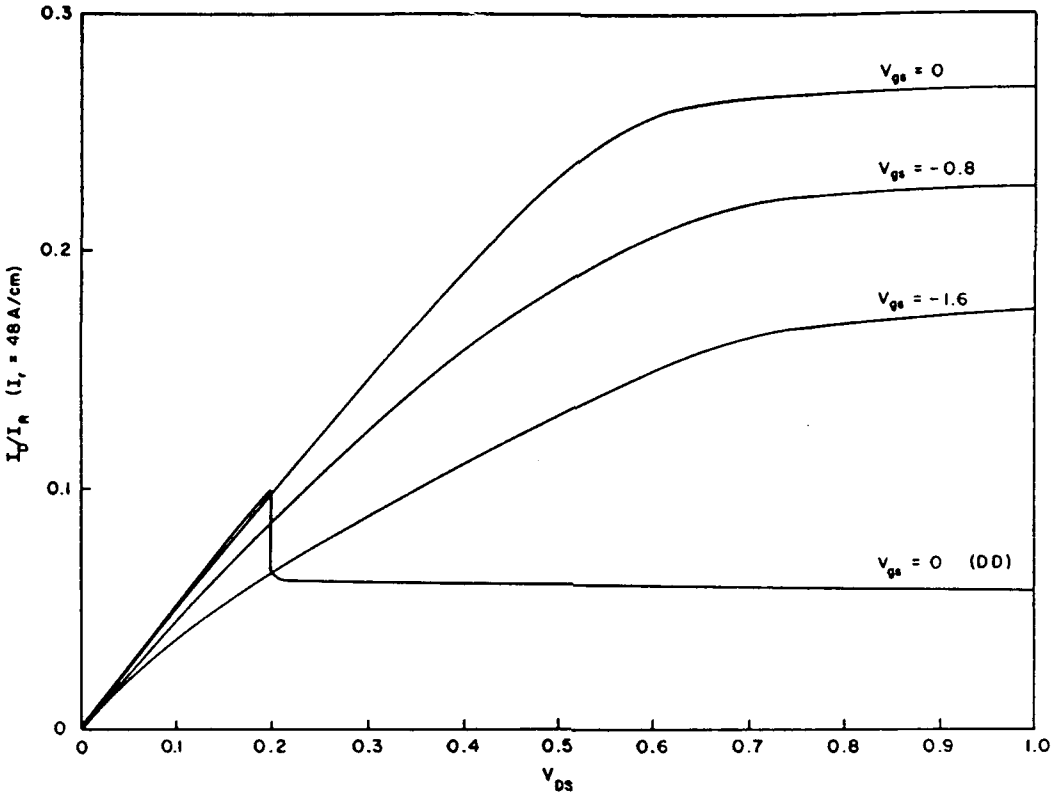


Figure 55. Current vs. drain voltage for OGST from MBTE simulation. DD results shown for $V_{gs} = 0$ for comparison.

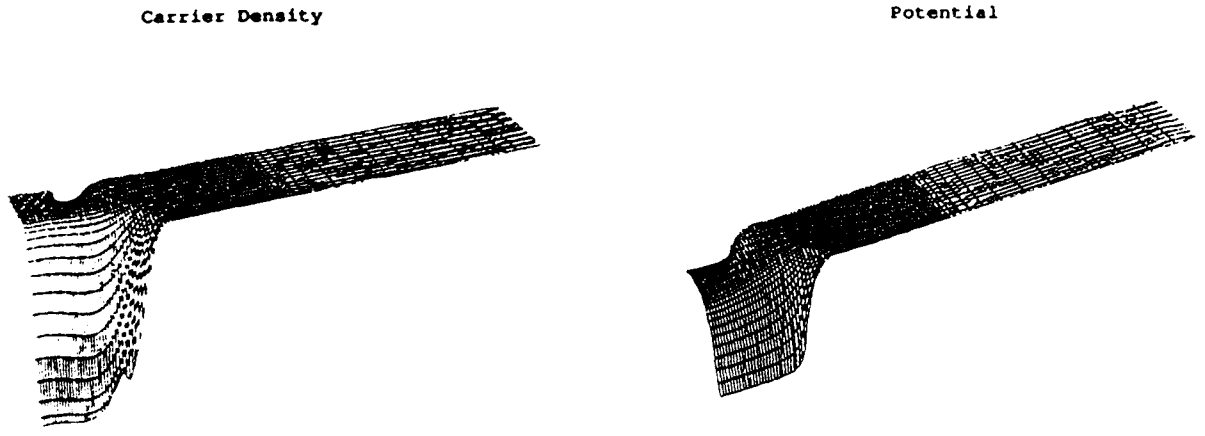


Fig. 56. Carrier density and potential distributions in OGST at $V_{ds} = 0.5$ volts and $V_{gs} = 0$ volts as predicted from MBTE simulations.

Similar characteristics are observed in the potential distribution. The field normal to the source contact is rather flat, as in the high current DD result, however the remainder of the potential distribution appears similar to the low current DD result (see Fig. 54).

The small signal unity gain cut off frequency, f_T, was also computed using the MBTE simulation procedure. The results are shown in Fig. 57. For $V_{ds}=0.5$ volts see that the curve of f_T vs V_{gs} is relatively flat, varying from an f_T of 128 GHz to and f_T of 211 GHz. At $V_{ds}=0.75$ there is considerably more variation with f_T ranging from 37 GHz to 240 GHz. The sharp reduction in f_T at $V_{ds}=0.75$ compared to the $V_{ds}=0.5$ value, for $V_{gs}=0$ is due to a factor of 3.5 reduction in the transconductance. Similarly, the increase at $V_{gs}=-1.6$ is due to an increase in transconductance.

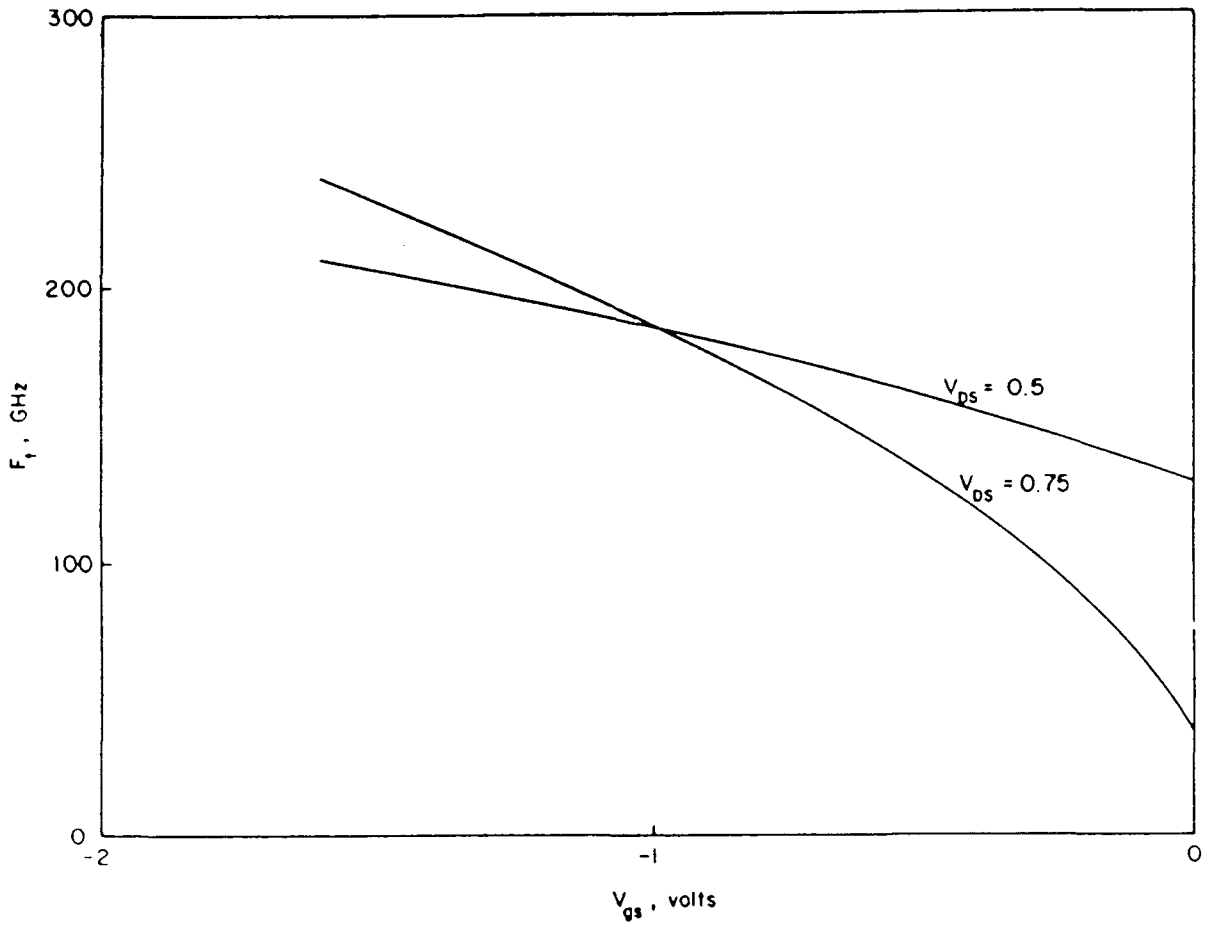


Figure 57. Unity gain cutoff frequency, F_t as a function of gate bias for OGST as predicted from solutions of MBTE.

Finally, a transient switching calculation was performed using the MBTE. The initial condition for the transient was chosen as the $V_{ds} = 0.75$ volt, $V_{gs} = -0.8$ volt bias point. The gate was then switched to -1.6 volts. The transient response at the device contacts is shown in Fig. 58 for 17 psec following the change in the gate bias. From this result it is apparent that the current transient lasts only about 6 psec with the major aspects of the response occurring in less than 1 psec. The response during the first psec is shown on an expanded scale in Fig. 59. Here we observe an initial drop in the gate current, due to displacement effects, accompanied by increases in the source and drain. We note that positive current at the source and drain indicate electrons leaving the device and negative currents, electrons entering. Thus, the initial increases in the drain and source current are a result of the explosion of electrons from the device as a new, larger depletion region is established at the gate. As the transient continues, the drain current decays relatively smoothly with only a small under shoot, to its new dc level. An oscillatory behavior is observed at the source and gate. This oscillatory behavior is due in part to the inertia of the electrons and, combined with the displacement effects at the gate, give rise to an RLC oscillation between the source and gate which damps by about 0.75 psec.

The results of these simulations further support those of Krusius and Berenz [7], namely that the OGST is a device with excellent potential for millimeter-wave operation. From the simulations reported here it would appear that, through careful design and analysis, an OGST with a unity gain cutoff frequency in excess of 100 GHz could be fabricated. However, it must be cautioned that while it is quite easy to conceptualize and simulate such a device, fabrication will pose many new and challenging problems. Clearly, additional work should be done at the simulation level to investigate the effects of assymetrices in the device structure, since the positive attributes of this device are largely due to its symmetric operation.

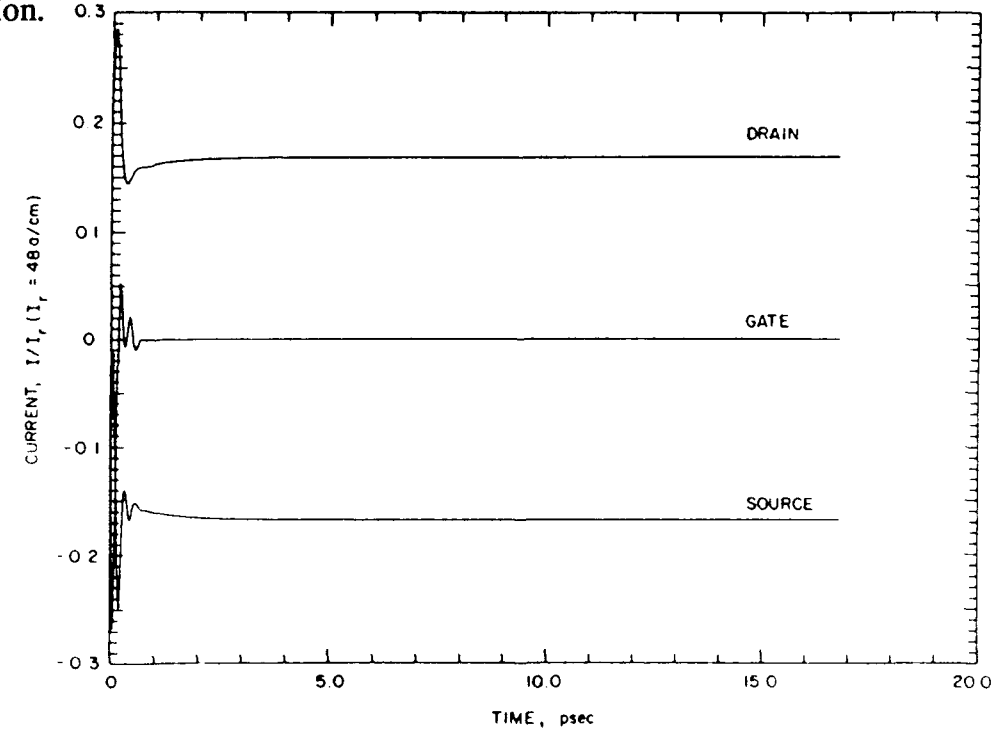


Figure 58. Transient current response for OGST when switching gate from -0.8 volts to -1.6 volts. V_{ps} = 0.75 volts.

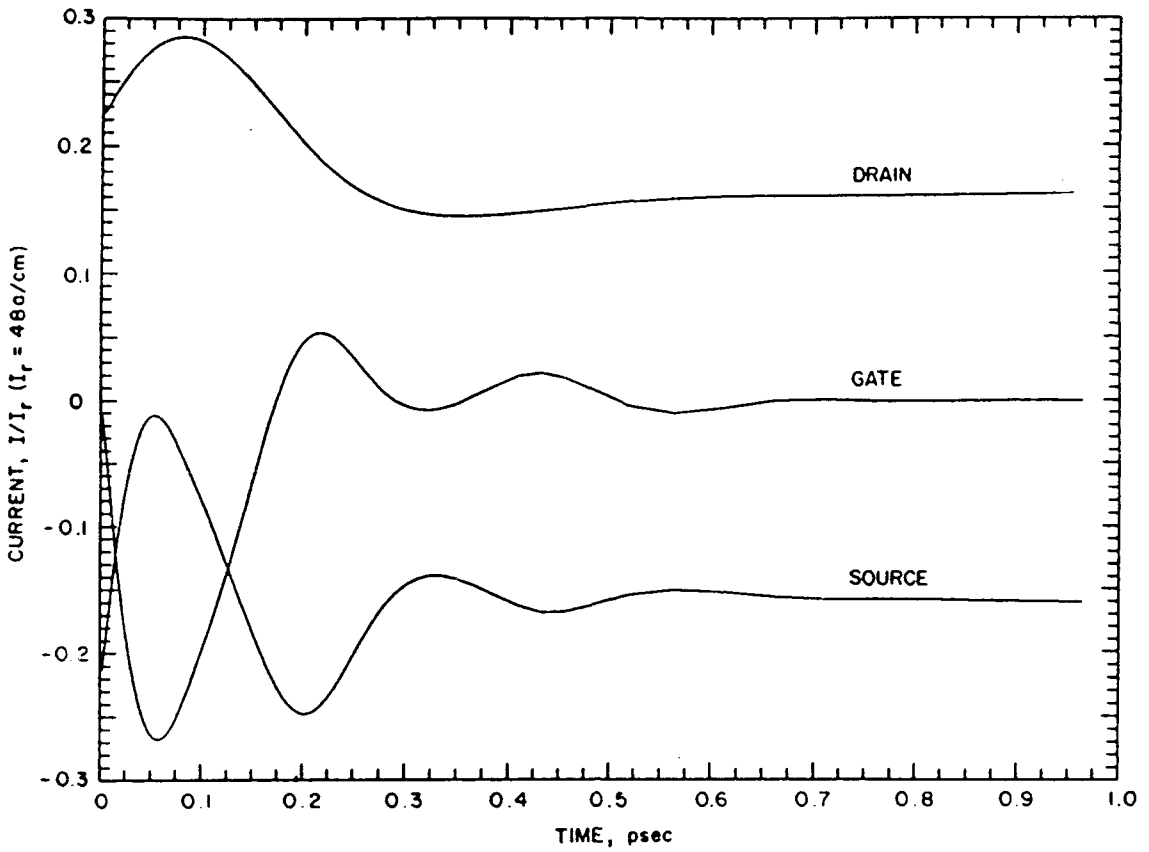


Figure 59. Transient current response for OGST when switching gate from -0.8 volts to -1.6 volts. V_{ps} = 0.75 volts.

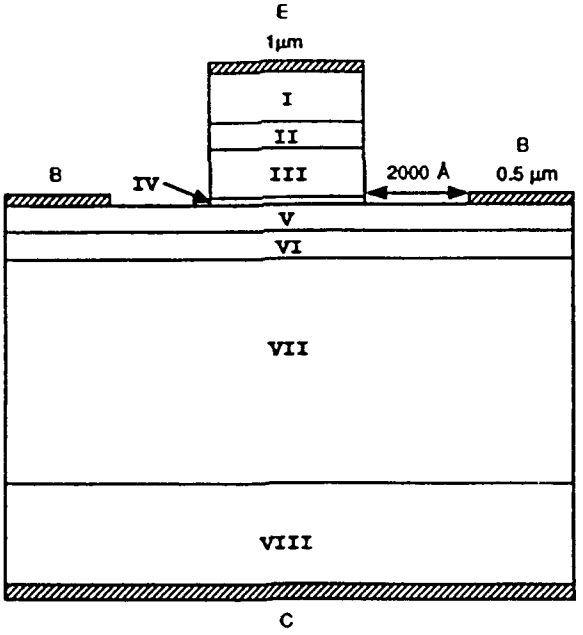
IV.3 HETEROSTRUCTURE BIPOLAR TRANSISTOR CALCULATIONS

Heterostructure bipolar transistors have received wide attention for high frequency applications. The InP/InGaAs material system offers many advantages over the AlGaAs/GaAs system. Particularly noteworthy is the low surface recombination of the In based materials. In addition, the higher saturation velocity of InP over GaAs is a significant factor in collector transport. The higher low field electron mobility of InGaAs over GaAs is significant in reducing base transit time. The valence band discontinuity of InP/InGaAs combination is about six times higher than that of the popular rival AlGaAs/GaAs material system.

The above advantages are expected to result in higher frequencies and current gain than the figures-of merit achieved for AlGaAs/GaAs HBTs. Hence there is a need to understand the physics of operation of the InP-based HBTs. With this in mind, two-dimensional simulations have been performed to understand HBT device transport. The analysis was based on solutions to the drift and diffusion equations and the Poison's equation as outlined in earlier sections. Quasistatic fields arising from band variations in heterostructures have been included in the definition of carrier currents. Field-dependent and density-dependent mobilities and diffusivities were used to describe the electron transport.

Prior to this study, at SRA we have performed extensive investigations on AlGaAs/GaAs HBTs. Our previous experience with self aligned AlGaAs/GaAs HBTs indicates that a bandgap grading must be employed in order to sweep the electrons across the base. In the absence of such grading, the dominant mechanism for base transport in diffusion. In self aligned structures, we found that due to the close proximity of the emitter and base contact edges, electrons diffuse toward the base contact resulting in current spreading and lower current gains. Based on this experience, we have employed bandgap grading of the base region since the emitter edge and base contact are separated only by 2000Å.

The goal of the investigation was to understand the device operation of the In based HBTs. In addition, advantages of double-heterostructure vs. single heterostructure HBTs were examined. The results are discussed below. Fig. 61 shows the variation of collector current with base voltage for the structure shown in Fig. 60. The collector bias is fixed at V_{CE} = 2.0V throughout this study. Using a basis of 1 A/cm^2 for the device turn-on, the turn-on voltage is determined to be 0.415V. Such a small value is a consequence of the narrow bandgap of $In_{0.53}Ga_{0.47}As$(E_g = 0.75ev). In contrast, the reported turn-on voltage for the AlGaAs/GaAs HBTs is approximately 1.0 volt. The highest collector current density computed here is $I_c = 1x10^5$ A/cm^2 at V_{BE} = 1.0v.



(I)	EMITTER CAP	$In_{0.53}Ga_{0.47}As$	1000 Å	5 x 10^{18} N$^+$
(II)	GRADED LAYER	InGaAs → InP	500 Å	5 x 10^{18} N$^+$
(III)	EMITTER	InP	1000 Å	2 x 10^{17} N
(IV)	GRADED LAYER	InP → InGaAs	100 Å	2 x 10^{17} N
(V)	BASE	BANDGAP GRADING $In_{0.53}Ga_{0.47}As$	500 Å	5 x 10^{18} P$^+$
(VI)	GRADED LAYER	InGaAs → InP	500 Å	1 x 10^{17} N
(VII)	COLLECTOR	InP	4500 Å	1 x 10^{17} N
(VIII)	SUBCOLLECTOR	$In_{0.53}Ga_{0.47}As$	2000 Å	5 x 10^{18} N$^+$

Figure 60. Schematic of the InP/InGaAs/InP HBT.

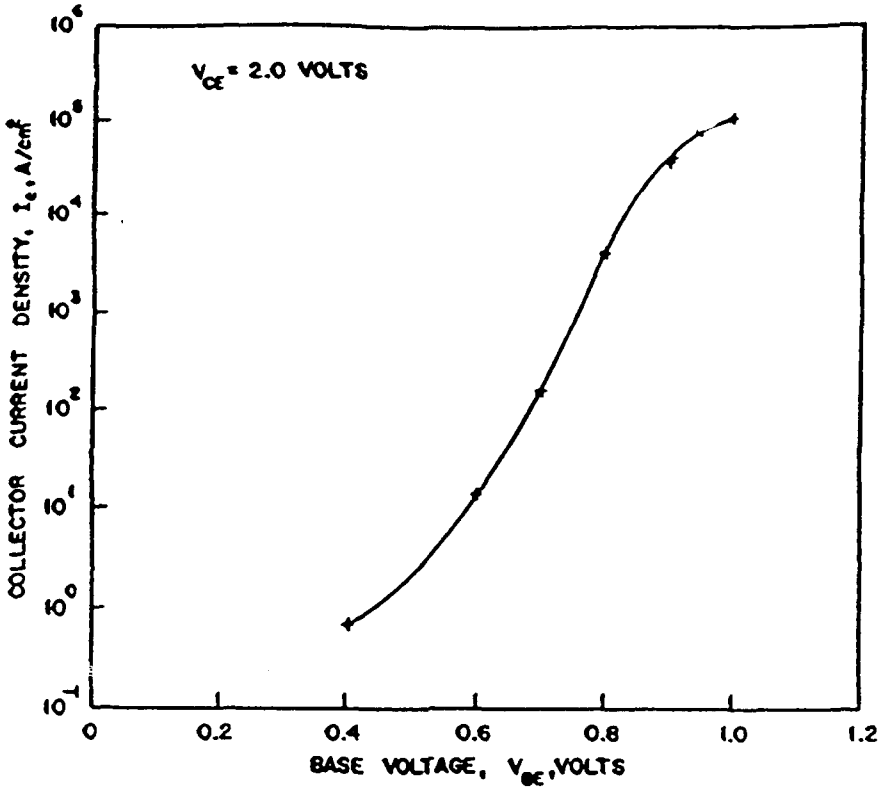


Figure 61. Collector current vs. base voltage at V_{ce} = 2.0v.

For purposes of comparison and interpretation we performed a set of computations with an InGaAs collector, i.e. layers VI and VII in figure 60 were replaced with $In_{0.53}Ga_{0.47}As$. With this modification, there is no heterostructure at the base/collector junction; hence no conduction band spike common to the double heterostructures. Such a direct comparison would enable us to understand the effects of the conduction band spike on collector transport. The I_C vs V_{BE} variation for the structure with the InGaAs collector (hereafter called the SHBT for single heterostructure) is identical to that of the DHBT in the scale used in Fig. 61. This is due to the fact that the collector current is determined by the emitter/base injection characteristics which are the same in both cases. Fig. 62 shows the electron density profile in the center of the device at a representative bias of V_{BE} = 0.7V. The profiles are nearly identical in the emitter and base regions for the two cases but show differences in the collector. Since the saturation velocity of InP is higher than InGaAs by a factor of three, the electron density in the InP collector is smaller than that in InGaAs collector by the same factor.

Figure 63 shows the conduction band profile in the device from the emitter/base junction to the base/collector junction at V_{BE} = 0.7, 0.9 and 1.0 volts and V_{CE} = 2.0 volts. The corresponding profiles for the device with the InGaAs collector are also shown for comparison. The profiles for the SHBT and DHBT are identical in the emitter and the base since these characteristics do not change for these two structures. However, the collector characteristics are different as discussed above. The profiles for the InGaAs collector do not have any spike in the conduction band at the base/collector junction. For the InP collector, the conduction band at thermal equilibrium (not shown here) does not display any spike since the heterojunction is graded to eliminate the spike. At low bias and current levels, this characteristic is maintained; however, as the collector current increases,

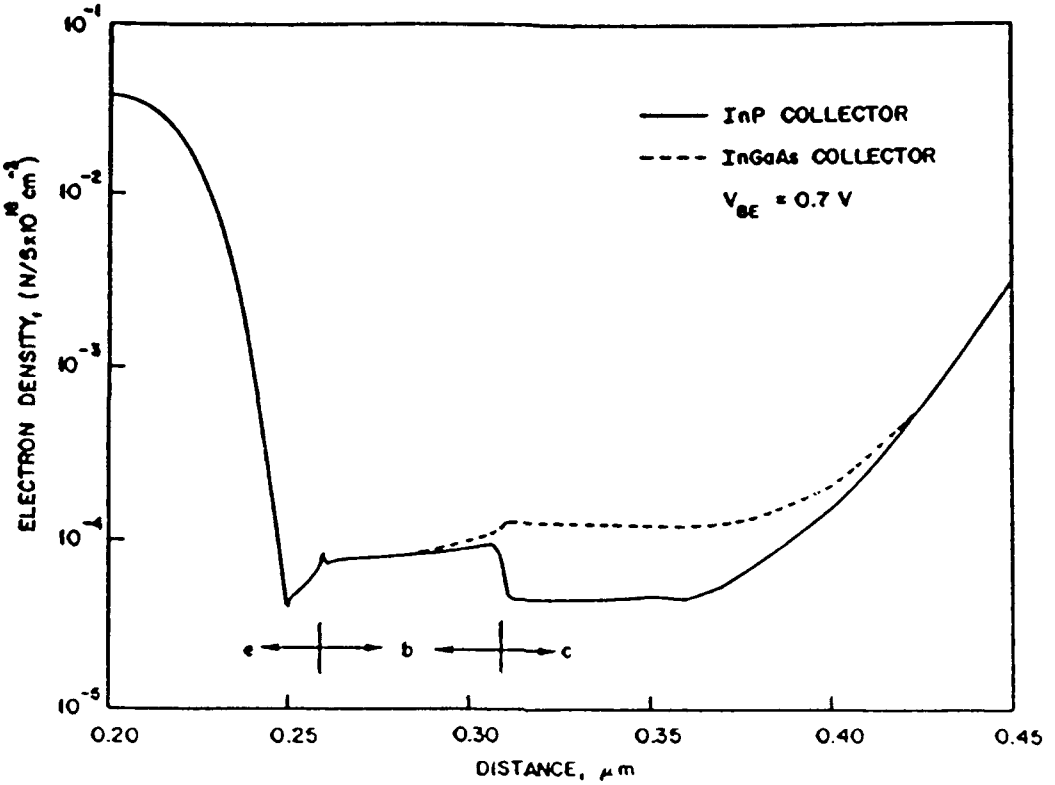


Figure 62. Electron density profile, V_{be} = 0.7 v.

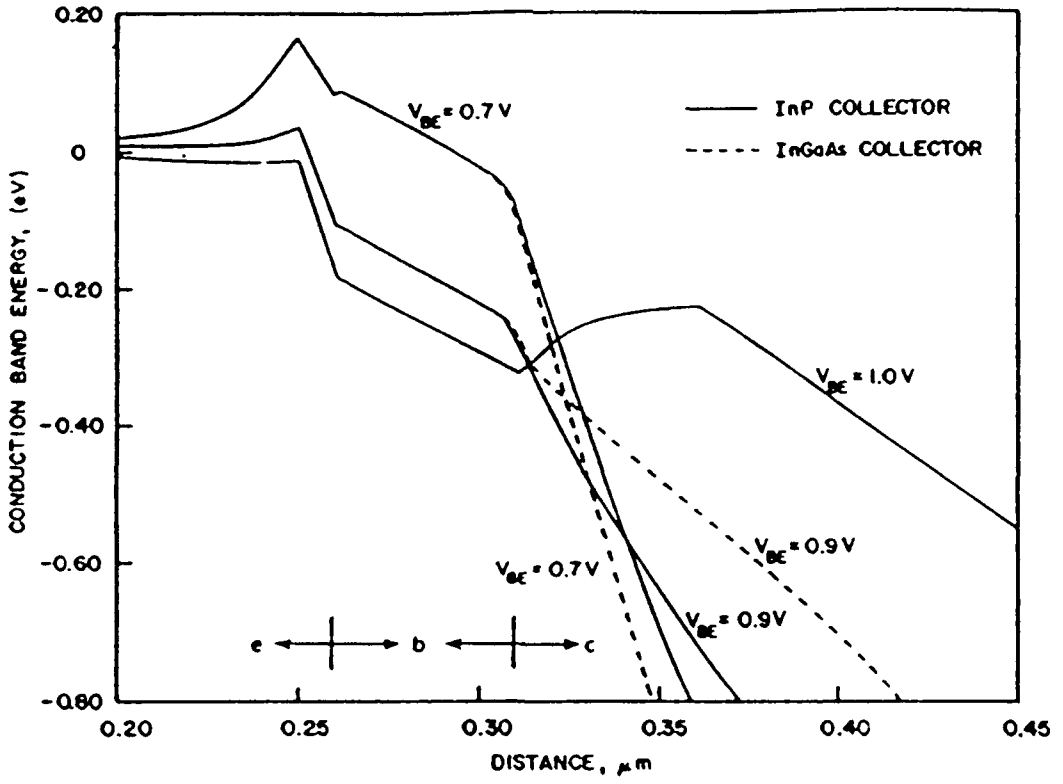


Figure 63. Conduction band diagram.

the spike reappears at the base/collector junction (see the curve at V_{BE} - 1.0V). Such observations have been made and explained by Tiwari [8] for AlGaAs/GaAs/AlGaAs double heterostructures. Tiwari [8] has shown that the reappearance of the spike at high collector current levels is detrimental to the efficient collection of electrons; in addition, the base current increases rapidly, resulting in poor gains. In [8], the above phenomenon was shown to occur at collector current densities above 1 x 10^4 A/cm^2 for the AlGaAs/GaAs/AlGaAs DHBT. The bounds on the current level for the occurrence of this phenomenon are dependent on the collector doping and nature of compositional grading. Longer grading widths and higher dopings may alleviate the problem to some extent. However, in the present investigation, the spike in the conduction band reappears only at voltages above 0.95V and I_c above 8 x 10^4 A/cm^2. Hence, it is not considered to be a serious problem. If the graded layer in Fig. 60 was smaller than 500 Å, this phenomenon is likely to occur at lower current densities.

The computed dc current gain from DDE simulation for the DHBT shows a peak of 26300 at I_c = 3.8 x 10^4 A/cm^2. At higher currents, the gain decreases. The cut-off frequency variation with the collector current for the DHBT is shown in Fig. 64. The maximum f_T computed is 78.6 GHz at I_c = 5.51 x 10^4 A/cm^2. In comparison, when the collector is InGaAs, the maximum f_T is only 46.9 GHZ. The InGaAs collector is not only inherently slower but also lowers the breakdown voltage due to its narrow bandgap. In comparing against the AlGaAs/GaAs HBTs, the InP/InGaAs HBTs offer more promise for high frequency performance. Similar DDE numerical simulations for a nearly optimized AlGaAs/GaAs HBT [9] showed a maximum f_T of 63.4 GHz. The structure in Fig. 60 is not optimized; an optimization of layer widths and doping is likely to yield a higher f_T.

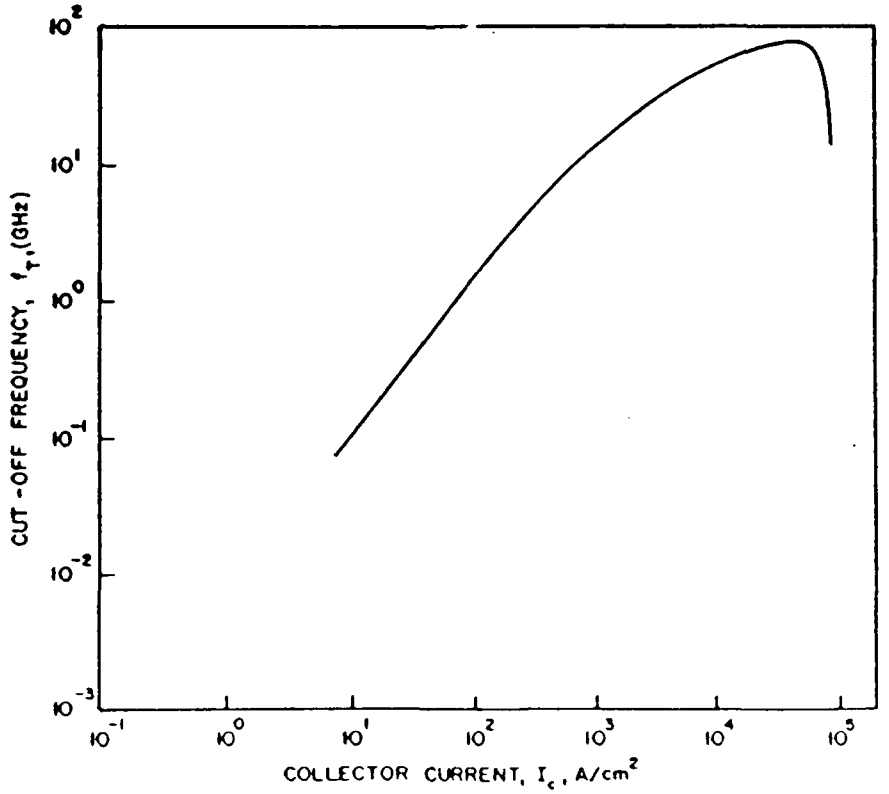


Figure 64. Variation of f_T with collector current.

The above results of the study were presented at the First International Conference on InP and Related Materials and subsequently published in the Proceedings. This publication is enclosed here. The conclusions of this study are that the InP-based HBTs have more promise than GaAs HBTs in terms of high frequency performance. The double-heterostructure (InP/InGaAs/InP) HBT is better than single heterostructure (InP/InGaAs/InGaAs) HBT in terms of high frequency performance and break-down characteristics.

In a companion study, we have also evaluated the high frequency performance of InP-based HBTs through transient solutions to the governing equations. Traditionally, the maximum frequency of oscillation f_{max} is taken to be $(f_T/8\pi r_b C_c)^{0.5}$. Here r_b is the base sheet resistance and C_c is the capacitance. This formula is often inaccurate. For this reason, we have chosen to compute f_{max} through transient solutions to the governing equations. The procedure involves determination of the Y-parameters and can be briefly described as follows. Perturbing the voltage on one contact while holding all other voltages constant, produces a response in current at the contacts. This response is calculated and used to derive the y-parameters via performing Fourier transforms.

A series of computations were performed by varying the base voltage at a constant collector bias of 2.0 volts. The Gummel plot generated from this (not shown here) has an ideality factor of unity. The maximum I_c is about 10^5 A/cm^2. The turn-on voltage is computed to be about 0.5 v with 1 A/cm^2 used as a basis. This is higher than the values reported in our previous study [10] for devices with lower base doping. Base doping of the order 5 x 10^{19} or above currently used in HBTs to reduce the base resistance, increases the barrier at the emitter/base junction and raises the turn-on voltage. The maximum dc current gain computed for this structure is 8000.

Figure 65 shows a conduction band diagram at V_{BE} = 1.0v and V_{CE} = 2.0v. The interesting feature here is that there is no spike seen at the base/collector junction at 1.0 volts with the introduction of the graded layer. Tiwari [8] showed that a spike in the conduction band reappears (even with collector grading) at high base voltages and collector currents and this phenomenon is detrimental to the efficient collection of electrons. We have also shown in our previous studies with lower base dopings ($5x10^{18}p^+$) that the reappearance of the spi occurs at about 0.95 voltage. The present computations reveal that an increase in base doping delays this phenomenon. The high frequency performance of the device is shown in figure 66. The highest f_{max} obtained here is 190 GHz at a current density of about $1.5x10^4$ A/cm^2. The highest f_T here is 40 GHz. The structure is not fully optimized and hence, it is entirely possible to obtain higher frequencies. In the entire operating range, the f_{max} is higher than f_T by a factor of two (ie.$f_{max} > 2f_T$).

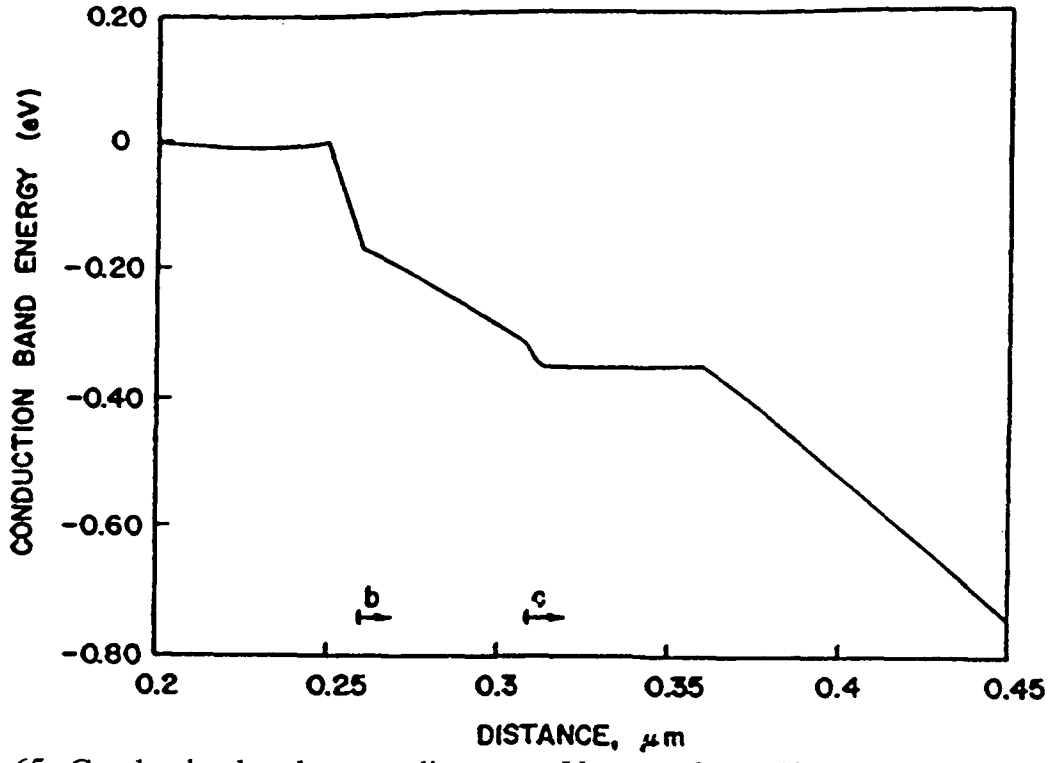


Figure 65. Conduction band energy diagram at V_{be} = 1.0 v and V_{ce} = 2.0 v.

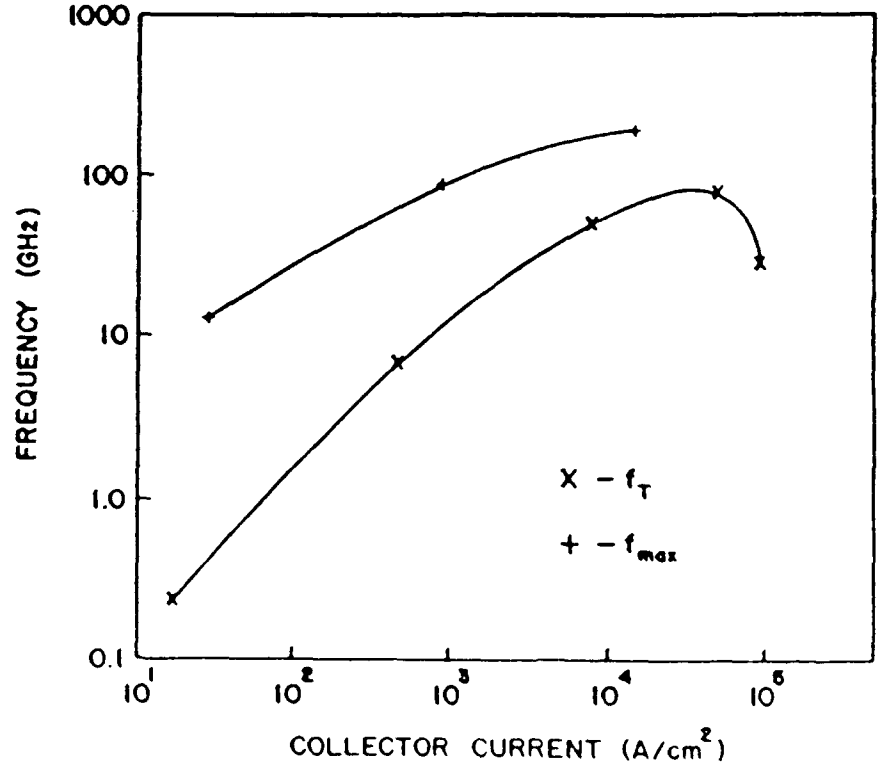


Figure 66. f_T and f_{max} vs. collector current.

The numerical studies undertaken here indicate the InP-based HBTs have significant promise for high frequency applications. They are capable of delivering high current, and speed for various digital and analog applications. We recommend the following for future work. (1) The limited scope of the present work excluded the investigation of InP based HBTs for power performance. This must be done in the future. Optimization with regard to emitter pattern size, doping and layer thickness must be undertaken for high speed and power performance. In addition, breakdown characteristics need to be obtained. (2) P-N-P structures for complementary device circuits would be appropriate; currently there is no information on this structures. (3) For switching applications, circuit simulations incorporating the 2-D models of the type presented here are needed to compute switching times taking into account various parasitics.

The results of this study were presented at the Second International Conference on InP and Related Materials and subsequently published in the proceedings. This publication is enclosed here.

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APPENDIX

Publication resulting in part from funding under this contract.

P27

Analysis of InP/InGaAs Double Heterostructure Bipolar Transistors for High Frequency Applications

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Abstract

The results of a two dimensional simulation of an InP/InGaAs double heterostructure bipolar transistor are discussed. High frequency performance is evaluated from transient solutions to the governing equations. The computed f_{max} is larger than twice the f_T over a wide range of collector current.

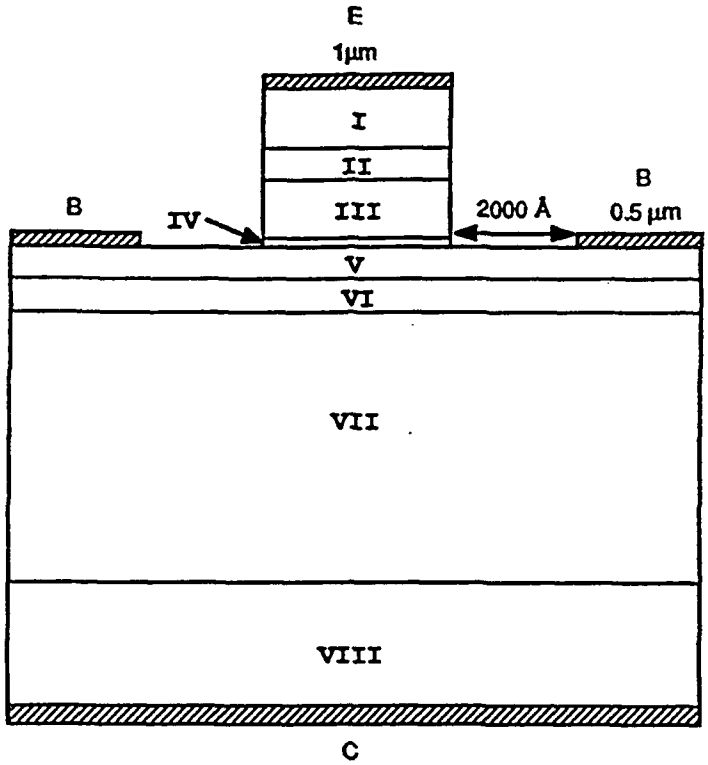
Introduction

The indium phosphide based heterostructure bipolar transistor, (HBT) has been considered to be a suitable candidate for high frequency applications. A combination of desirable transport properties and band discontinuities makes the InP/InGaAs HBTs more attractive than their counterparts in the AlGaAs system. Use of wide band gap InP as a collector material instead of InGaAs provides fast collector transit times and high break down voltages. In an earlier work [1] we presented the physics of an InP/InGaAs/InP double heterostructure bipolar transistor (DHBT) and also compared InP vs InGaAs as collector materials. In the present study, we provide an analysis for the high frequency performance of InP DHBTs. In particular, the maximum frequency of oscillation f_{max} is computed from transient solutions to the governing equations rather than from approximate formulas widely used.

Analysis

Figure 1 shows a representative InP/InGaAs/InP DHBT analyzed in the present study. Graded layers have been used at the cap/emitter, emitter/base and base/collector junctions. In addition, bandgap grading is employed in the base region. Our previous experience [2] with self aligned AlGaAs/GaAs HBTs indicated that bandgap grading helps to sweep the electrons across the base. In the absence of such grading, the dominant mechanism for base transport is diffusion. In self aligned structures, we found that due to the close proximity of the emitter and base contact edges, electrons diffuse toward the base contact resulting in current spreading and lower current gains. Grading the bandgap in the base alleviates this problem while it also improves the base transit time. The dimensions of various layers and doping levels are given in figure 1.

The governing equations considered in this study are the drift and diffusion equations and Poisson's equation. Quasi-fields arising from band variations in heterostructures have been included in the definition of carrier current. Field and density dependent mobilities and diffusivities were used to describe carrier transport. The details can be found in ref. [2]. This analysis does not include nonequilibrium transport which would require solutions to



(I)	EMITTER CAP	$In_{0.53}Ga_{0.47}As$	1000 Å	5×10^{18} N^+
(II)	GRADED LAYER	InGaAs → InP	500 Å	5×10^{18} N^+
(III)	EMITTER	InP	1000 Å	2×10^{17} N
(IV)	GRADED LAYER	InP → InGaAs	100 Å	2×10^{17} N
(V)	BASE	BANDGAP GRADING $In_{0.53}Ga_{0.47}As$	500 Å	2×10^{19} P^+
(VI)	GRADED LAYER	InGaAs → InP	500 Å	1×10^{17} N
(VII)	COLLECTOR	InP	4500 Å	1×10^{17} N
(VIII)	SUBCOLLECTOR	$In_{0.53}Ga_{0.47}As$	2000 Å	5×10^{18} N^+

Fig. 1. Schematic of the HBT

the moment equations or a Monte-Carlo simulation.

To assess high frequency performance, we have computed f_T and f_{max}. It is noted that f_{max} is usually computed using the approximate formula $f_{max} = (f_T/8\pi r_b C_c)^{0.5}$. However, it has been recently shown [3] that this formula is inaccurate, especially at high current levels. In the present study, we compute f_{max} from transient accurate solutions. The procedure involves determination of the Y-parameters and is outlined below [4]. Perturbing the voltage on one contact while holding all other voltages constant, produces a response in current at another contact. This response is calculated and used to derive the y-parameters via performing Fourier transforms and utilizing the following relation:

$$\tilde{Y}_{jk} = \frac{F\{i_j(t) - I_j(o)\}}{F\{V_k(t) - V_k(o)\}},$$

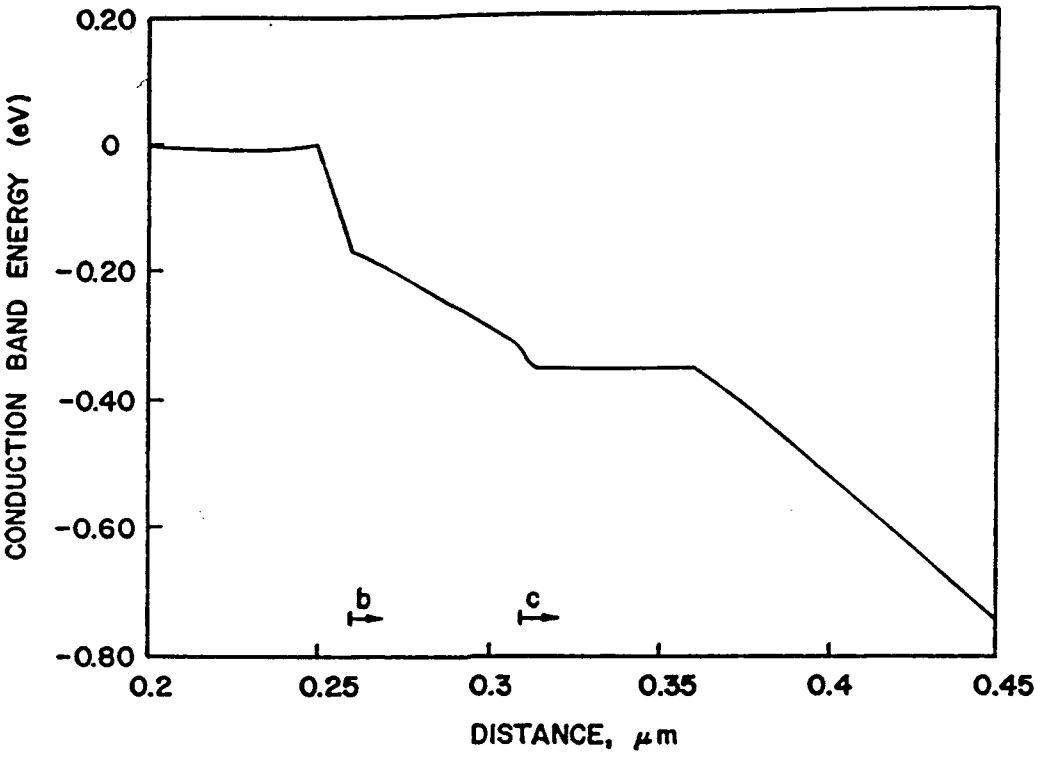


Fig. 2. Conduction Band Energy Diagram at $V_{BE}=1.0v$ and $V_{CE}=2.0v$

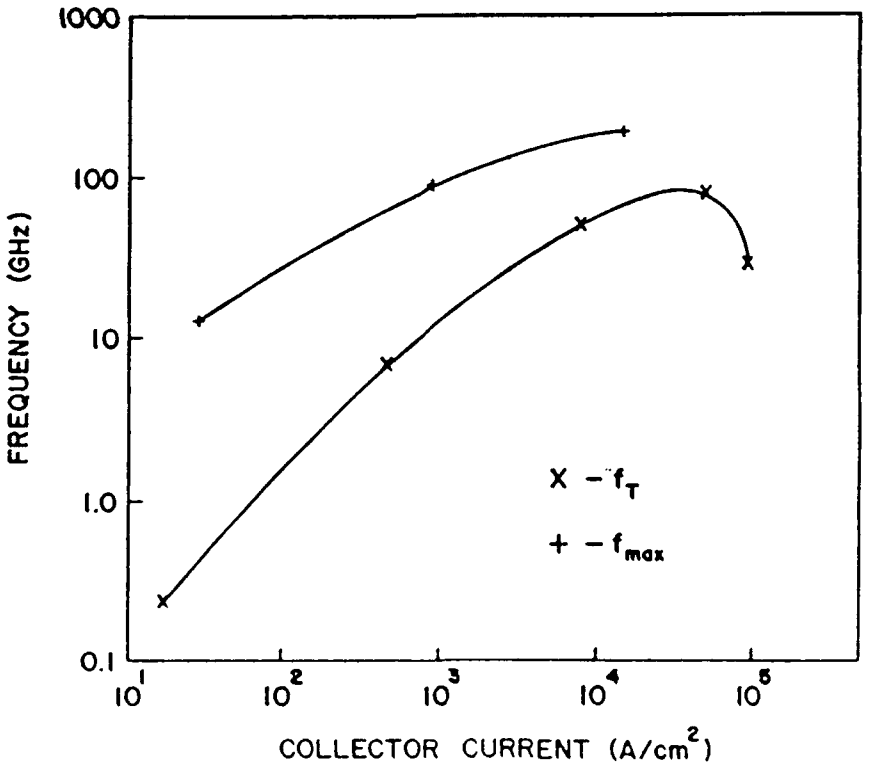


Fig. 3. f_T and f_{max} vs Collector Current

where $i_j(t)$ and $v_k(t)$ are the total current and total voltage at time t at contact j and contact k, respectively; and $I_j(o)$ and $v_k(o)$ are the initial current and voltage at contact j and k, respectively. F denotes the Fourier transform operator, and the tilde implies a complex number. The value of f_{max} is obtained by determining the frequency at which the maximum available gain (which is a function of the y-parameters) becomes unity.

A series of computations were performed by varying the base voltage at a constant collector bias of 2.0 volts. The Gummel plot generated from this (not shown here) has an ideality factor of unity. The maximum I_c is about 10^5 A/cm^2. The turn-on voltage is computed to be about 0.5v with 1 A/cm^2 used as a basis. This is higher than the values reported in our previous study [1] for devices with lower base doping. Base doping of the order 5×10^{19} or above currently used in HBTs to reduce the base resistance, increases the barrier at the emitter/base junction and raises the turn-on voltage. The maximum dc current gain computed for this structure is 8000.

Figure 2 shows a conduction band diagram at V_{BE} = 1.0v and V_{CE} = 2.0v. The interesting feature here is that there is no spike seen at the base/collector junction at 1.0volts with the introduction of the graded layer. Tiwari [5] showed that a spike in the conduction band reappears (even with collector grading) at high base voltages and collector currents and this phenomenon is detrimental to the efficient collection of electrons. We have also shown in our previous studies with lower base dopings ($5x10^{18}p^+$) that the reappearance of the spike occurs at about 0.95 voltage. The present computations reveal that an increase in base doping delays this phenomenon. The high frequency performance of the device is shown in figure 3. The highest f_{max} obtained here is 190 GHz at a current density of about $1.5x10^4$ A/cm^2. The highest f_T here is 40 GHz. The structure is not fully optimized and hence, it is entirely possible to obtain higher frequencies. In the entire operating range, the f_{max} is higher than f_T by a factor of two (ie. $f_{max} > 2 f_T$).

Summary

In conclusion, we have performed numerical simulations to understand the operational characteristics of the InP-based HBTs. Values of f_{max} as high as 190 GHz have been computed for unoptimized structures. Proper doping and compositional grading in the base and collector layers reduce the problem of the conduction band spike at high collector current densities.

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Physics of InP/InGaAs Heterostructure Bipolar Transistors for EHF Applications

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ABSTRACT

A detailed examination of the physics of the InP based heterostructure bipolar transistors is reported. The governing drift and diffusion and Poisson's equations are solved numerically in two dimensions. The results show current gain as high as 26300 and an f_T of 78.6 GHz for an InP/InGa As/InP double heterostructure. The electric field profiles from the simulation are used in an adjunct Monte Carlo procedure to assess the effects of velocity overshoot. The Monte Carlo results indicate a substantial reduction in base and collector transit times from the corresponding drift and diffusion equation (DDE) simulations.

1. INTRODUCTION

Heterostructure bipolar transistors in the InP/InGaAs system have been gaining much attention recently due to their promise for high frequency applications. The InP/InGaAs system offers certain advantages over the AlGaAs/GaAs system. These include (i) low surface recombination, (ii) higher electron saturation velocity of InP than GaAs which is a significant factor in collector transport, (iii) higher low field electron mobility of InGaAs over GaAs which is a significant factor in base transport, (iv) a larger valence band discontinuity (ΔE_v = 0.37ev) compared to the AlGaAs/GaAs system (ΔE_v = 0.057ev) which is significant in the prevention of hole injection into the emitter and (v) larger value for intervalley separation in InP than in GaAs. These advantages are expected to result in higher current gain and cut-off frequency for the InP/InGaAs HBT over their AlGaAs/GaAs counterparts.

In the case of the AlGaAs/GaAs system, several theoretical studies have appeared in the past to provide an understanding of the electrical characteristics of the device and also as a design aid[1,2]. Issues on velocity overshoot for this system have been addressed using one dimensional Monte Carlo studies[3,4]. For the InP/InGaAs system, the only theoretical work in the literature is a one-dimensional Monte Carlo study by Pelouard et al.[5]; the authors have used their results to fit an analytical model for the I-V curves. The present work provides a detailed investigation of the physics of the InP/InGaAs HBTs. Two-dimensional numerical simulation of a representative device structure has been performed through solutions of the drift and diffusion equations. Current gain and cut-off frequency have also been computed. The highest f_T computed is 78.6 GHz at a collector current density of 5.5×10^4 A/cm^2 for a double heterostructure. The electric field profiles from the DDE simulations have been used in a Monte Carlo procedure to assess the effects of intervalley electron transfer and velocity overshoot.

2. DEVICE STRUCTURE

Simulations have been performed for a representative InP/InGaAs/InP double heterostructure bipolar transistor shown in Fig. 1. It is noted that in the AlGaAs/GaAs system, most of the reported studies consider a narrow gap (GaAs) collector while double heterostructures are investigated for special advantages such as hole suppression into the collector during logic cycle operation but not for purposes of high frequency

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operation. In the AlGaAs/GaAs system, wide gap collectors are not expected to yield higher f_Ts than the narrow-gap collectors[6] due to the lower drift velocit of AlGaAs than GaAs. In contrast, in the InP/InGaAs system, most of the reported studies are on double heterostructures since InP, with a high drift velocity of 1 x 10^7cm/s and a larger intervalley separation, qualifies as an excellent candidate for the collector material. A notable exception here is the work by Nottenburg et al.[7] who reported excellent f_Ts with an InGaAs colletor.

The dimensions of various layers and nominal doping levels are given in Fig. 1. Graded layers have been used at the cap/emitter, emitter/base, and base/collector junctions. In addition, band gap grading is employed in the base region. Our previous experience with self aligned AlGaAs/GaAs HBTs[8] indicates that a bandgap grading must be employed in order to sweep the electrons across the base. In the absence of such grading, the dominant mechanism for base transport is diffusion. In self aligned structures, we found that due to the close proximity of the emitter and base contact edges, electrons diffuse toward the base contact, resulting in a current spreading effect and lower current gains[8]. Based on this experience, we have employed bandgap grading in the base, since the separation between the emitter edge and the base contact is only 2000Å. However, it is recognized that achieving a linear grading of band gap in the InP/InGaAs system is not as straight forward as in the AlGaAs/GaAs system where the Al composition can be easily varied.

3. MODEL DETAILS

The governing equations considered in this study are the well known drift and diffusion equations and Poisson's equation. Quasi-static fields arising from band variations in heterostructures have been included in the definition of carrier currents. The details of the model can be found in ref. [2]. Field-dependent and density-dependent mobilities and velocities were used to describe the electron transport. These characteristics were obtained from Monte Carlo Calculations. The results from the DDE study provide the dc current gain β ($= I_c/I_b$) and cut-off frequency, f_T ($=g_m/2\pi C_T$) where g_m is the transconductance and C_T is the capacitance.

The DDE formulation does not include nonequilibrium transport. Hence, the DDE results do not reflect the benefits, if any, of velocity overshoot effects. In order to assess the effect of velocity overshoot on device performance and improve the utility of the DDE predictions, the following procedure was adopted. The details of electron transport across both the InGaAs base and InP collector were examined using an Ensemble Monte Carlo method. Initially the electrons were injected from the emitter-base junction (ΔE_c=100meV) with a hemi-Maxwellian energy distribution. These electrons were then moved, subject to the field profile obtained from the DDE results. The transfer of electrons from the InGaAs base to the InP collector was treated classically. Only those electrons, with kinetic energy associated with the perpendicular component of velocity exceeding the barrier height (ΔE=220meV), were allowed to transfer. The reflected electrons were reinjected again from the emitter-base junction. For the electrons which reach the collector contact, information about their energy, valley, and transit times was recorded. It is noted that the Monte Carlo computations here are not self-consistent; nevertheless they serve to highlight the inadequacies of the DDE simulation with respect to velocity overshoot in the base and collector regions.

4. DEVICE CHARACTERISTICS

Fig. 2 shows the variation of collector current with base voltage for the structure shown in Fig. 1. The collector bias is fixed at V_{CE} = 2.0V throughout this study. Using a basis of 1 A/cm^2 for the device turn-on, the turn-on voltage is determined to be 0.415V. Such a small value is a consequence of the narrow bandgap of $In_{0.53}Ga_{0.47}As$ (E_g=0.75ev). In contrast, the reported turn-on voltage for the AlGaAs/GaAs HBTs is approximately 1.0 volt. The highest collector current density computed here is I_c = 1 x 10^5 A/cm^2 at V_{BE} = 1.0v.

For purposes of comparison and interpretation we performed a set of computations with an InGaAs collector, i.e. layers VI and VII in figure 1 were replaced with $In_{0.53}Ga_{0.47}As$. With this modification, there is no heterostructure at the base/collector junction; hence no conduction band spike common to the double heterostructures. Such a direct comparison would enable us to understand the effects of the conduction band spike on collector transport. The I_c vs V_{BE} variation for the structure with the InGaAs collector (hereafter called the SHBT for single heterostructure) is identical to that of the DHBT in the scale used in Fig. 2. This is due to the fact that the collector current is determined by the emitter/base injection characteristics which are the same in both cases. Fig. 3 shows the electron density profile in the center of the device at a representative bias of V_{BE} = 0.7V. The profiles are nearly identical in the emitter and base regions for the two cases but show differences in the collector. Since the saturation velocity of InP is higher than InGaAs by a factor of three, the electron density in the InP collector is smaller than that in InGaAs collector by the same factor.

Figure 4 shows the conduction band profile in the device from the emitter/base junction to the base/collector junction at V_{BE} = 0.7, 0.9 and 1.0 volts and V_{CE} = 2.0 volts. The corresponding profiles for the device with the InGaAs collector are also shown for comparison. The profiles for the SHBT and DHBT are identical in the emitter and the base since these characteristics do not change for these two structures. However, the collector characteristics are different as discussed above. The profiles for the InGaAs collector do not have any spike in the conduction band at the base/collector junction. For the InP collector, the conduction band at thermal equilibrium (not shown here) does not display any spike since the heterojunction is graded to eliminate the spike. At low bias and current levels, this characteristic is maintained; however, as the collector current increases, the spike reappears at the base/collector junction (see the curve at V_{BE} = 1.0V). Such observations have been made and explained by Tiwari[9] for AlGaAs/GaAs/AlGaAs double heterostructures. Tiwari has shown that the reappearance of the spike at high collector current levels is detrimental to the efficient collection of electrons; in addition, the base current increases rapidly, resulting in poor gains. In refs. [6] and [9], the above phenomenon was shown to occur at collector current densities above 1×10^4 A/cm^2 for the AlGaAs/GaAs/AlGaAs DHBT. The bounds on the current level for the occurence of this phenomenon are dependent on the collector doping and nature of compositional grading. Longer grading widths and higher dopings may alleviate the problem to some extent. However, in the present investigation, the spike in the conduction band reappears only at voltages above 0.95V and I_c above 8×10^4 A/cm^2. Hence, it is not considered to be a serious problem. If the graded layer in Fig. 1 was smaller than 500 Å, this phenomenon is likely to occur at lower current densities.

The computed dc current gain from DDE simulation for the DHBT shows a peak of 26300 at $I_c = 3.8 \times 10^4$ A/cm^2. At higher currents, the gain decreases. The cut-off frequency variation with the collector current for the DHBT is shown in Fig. 5. The maximum f_T computed is 78.6 GHz at $I_c = 5.51 \times 10^4$ A/cm^2. In comparison, when the collector is InGaAs, the maximum f_T is only 46.9 GHz. The InGaAs collector is not only inherently slower but also lowers the breakdown voltage due to its narrow bandgap. In comparing against the AlGaAs/GaAs HBTs, the InP/InGaAs HBTs offer more promise for high frequency performance. Similar DDE numerical simulations for a nearly optimized AlGaAs/GaAs HBT[8] showed a maximum f_T of 63.4 GHz. The structure in Fig. 1 is not optimized; an optimization of layer widths and doping is likely to yield a higher f_T.

5. EFFECTS OF NONEQUILIBRIUM TRANSPORT

Since it is well known that velocity overshoot results in a reduction of the transit time, we have attempted to include its effects using a Monte Carlo procedure as outlined earlier. The resulting velocity profile for the electrons inside the device for the DHBT at V_{BE} = 0.7V and V_{CE} = 2.0V is plotted in Fig. 6 as a function of the distance from the emitter-base junction. Within the base region the velocity is highest due to the ballistic injection and the removal of the electrons reflected at the base/collector interface. These electrons are accelerated by the high field in the depletion layer and undergo transfer to the L-valley as can be seen

from the same figure. This leads to a smaller velocity for the electrons, even though some of the electrons return to the central valley in the neutral region of the collector where the field is low.

The velocities in the base and the collector in Fig. 6 are higher than the velocities from the DDE simulation which are essentially the corresponding saturation velocities at the fields encountered during device operation. Consequently, the transit time across the base and the emitter is smaller and the f_T is larger than the DDE predictions. For example, at $V_{BE} = 0.7V$ and $I_c = 154\ A/cm^2$, the f_T from DDE simulation is 2.5 GHz; the f_T computed using the shorter (base + collector) transit time from the MC simulation is 4.1 GHz. Note that at low current levels, the frequency characteristics are dominated by the emitter charging time; nevertheless we see a 64% improvement in f_T when overshoot is included. At higher current levels, when the base and collector transit times are dominant, consideration of velocity overshoot is expected to result in frequencies substantially higher than the predictions from DDE simulations. Additional calculations at high current levels and also for the SHBT wil be reported in the future.

6. CONCLUSIONS

A two dimensional numerical study has been used to obtain the device characteristics of an InP/InGaAs/InP heterostructure bipolar transistor. The simulations confirm the potential of InP/InGaAs HBTs for high frequency performance. An adjunct Monte Carlo study shows that nonequilibrium transport is indeed significant in the base and collector transport.

7. ACKNOWLEDGEMENT

This work was supported by DARPA and ONR.

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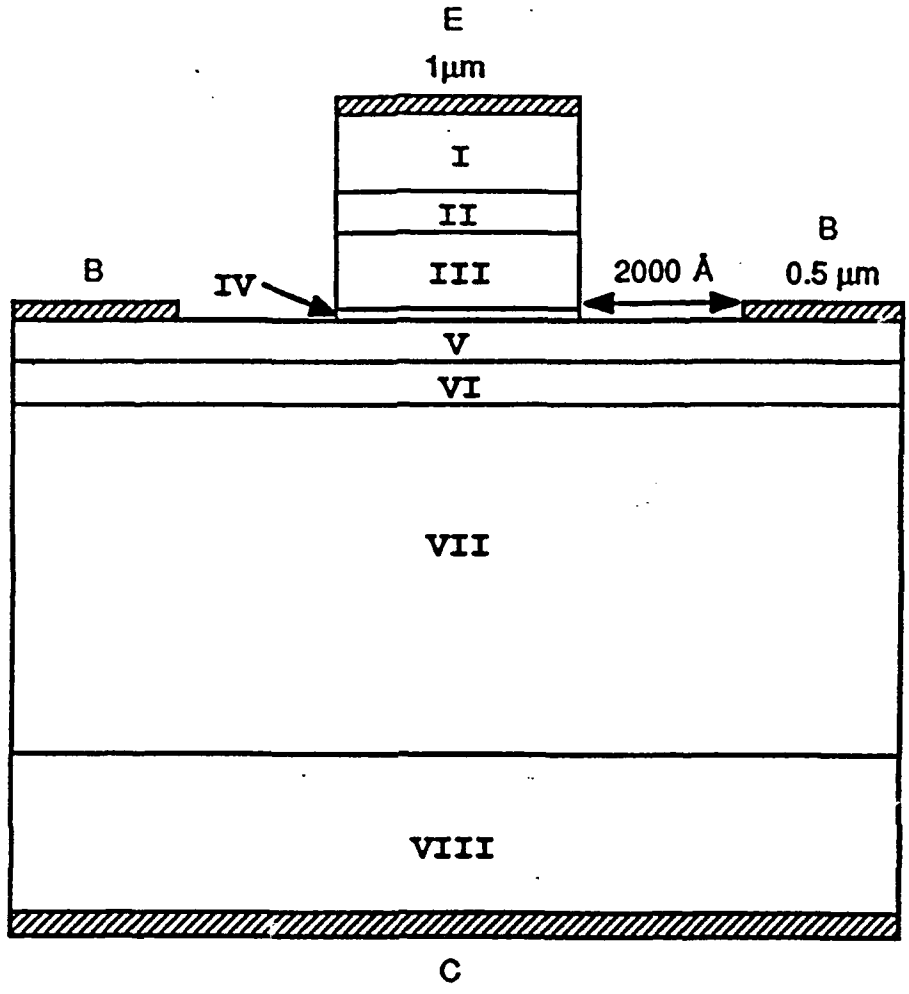

(I)	EMITTER CAP	$In_{0.53}Ga_{0.47}As$	1000 Å	5×10^{18} N^+
(II)	GRADED LAYER	InGaAs → InP	500 Å	5×10^{18} N^+
(III)	EMITTER	InP	1000 Å	2×10^{17} N
(IV)	GRADED LAYER	InP → InGaAs	100 Å	2×10^{17} N
(V)	BASE	BANDGAP GRADING $In_{0.53}Ga_{0.47}As$	500 Å	5×10^{18} P^+
(VI)	GRADED LAYER	InGaAs → InP	500 Å	1×10^{17} N
(VII)	COLLECTOR	InP	4500 Å	1×10^{17} N
(VIII)	SUBCOLLECTOR	$In_{0.53}Ga_{0.47}As$	2000 Å	5×10^{18} N^+

Figure 1. Schematic of the InP/InGaAs/InP HBT.

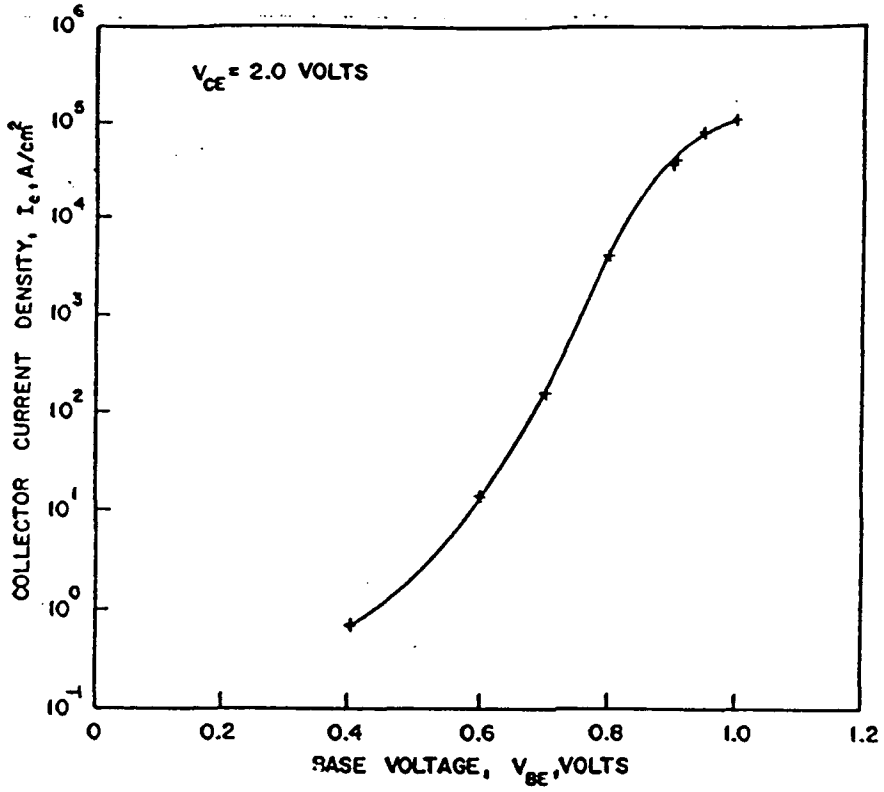

Figure 2. Collector Current vs. Base Voltage at V_{CE} = 2.0 v.

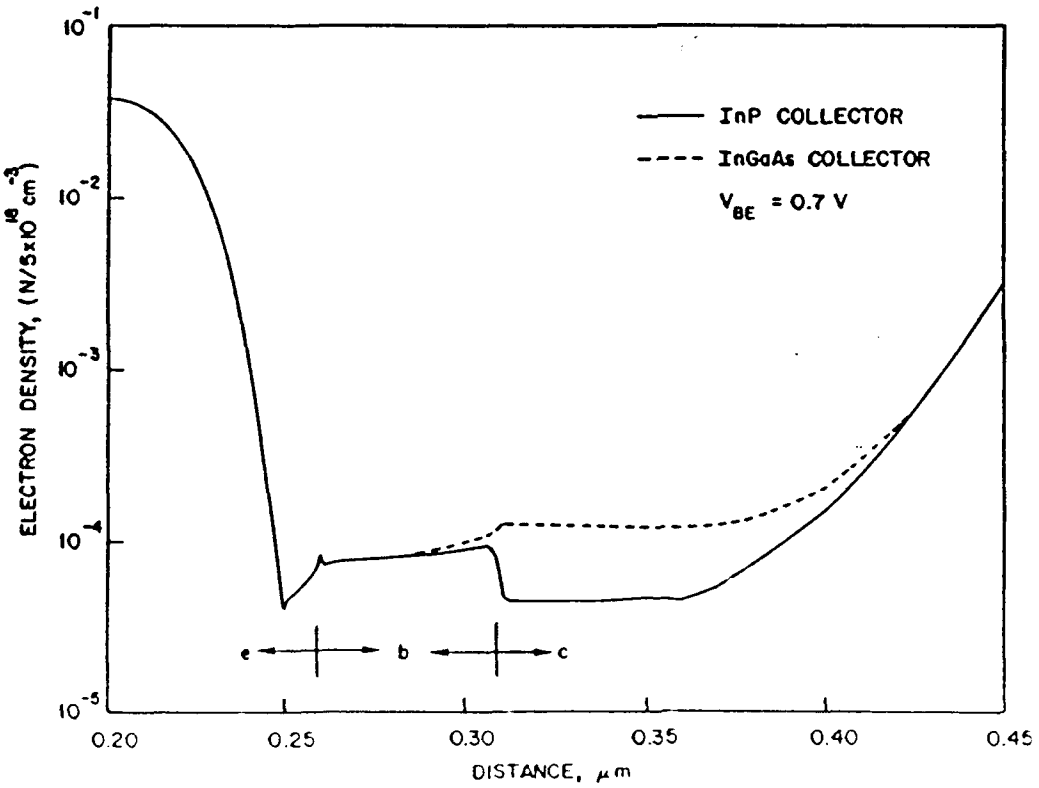

Figure 3. Electron Density Profile, V_{BE} = 0.7 v.

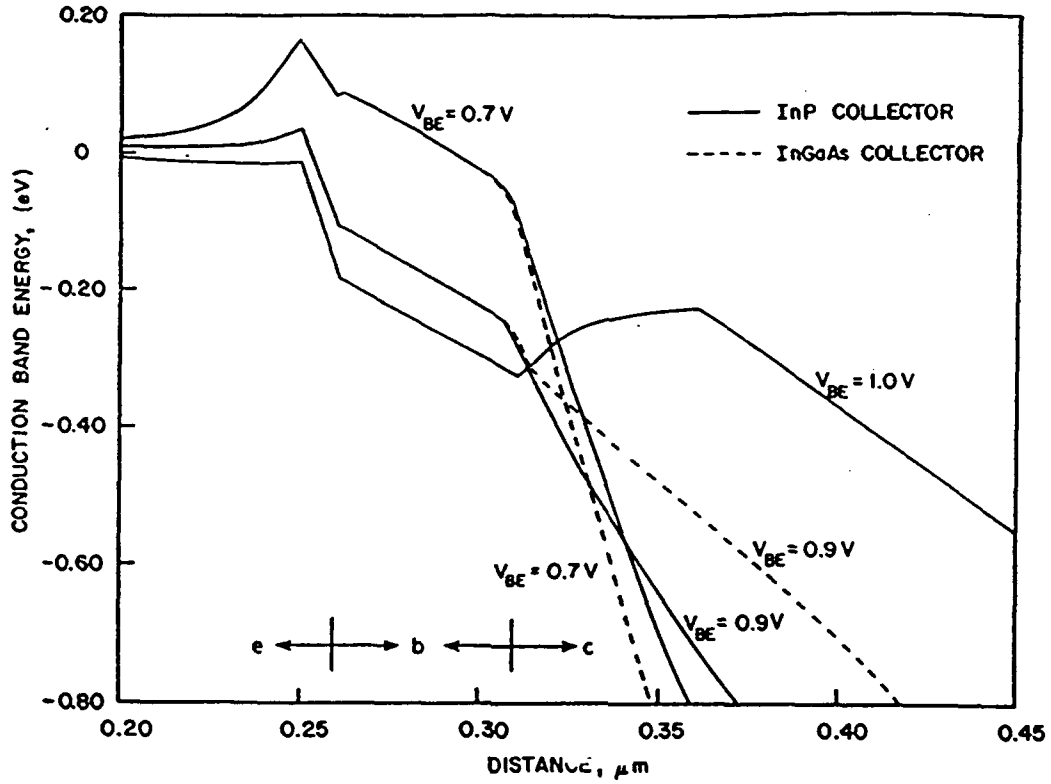

Figure 4. Conduction Band Diagram.

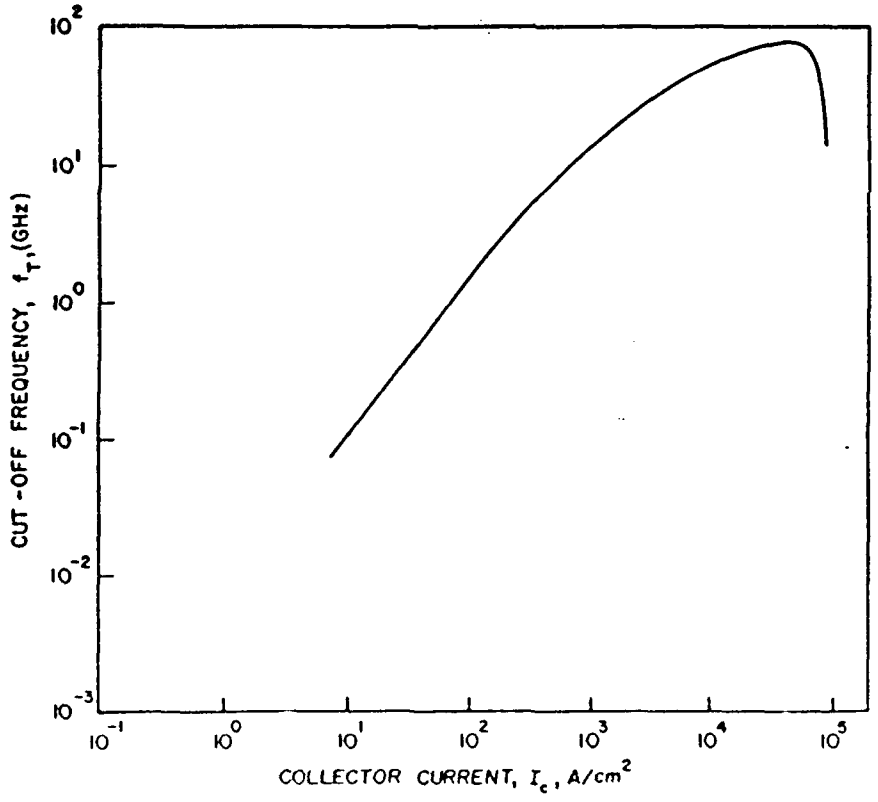

Figure 5. Variation of f_T with Collector Current.

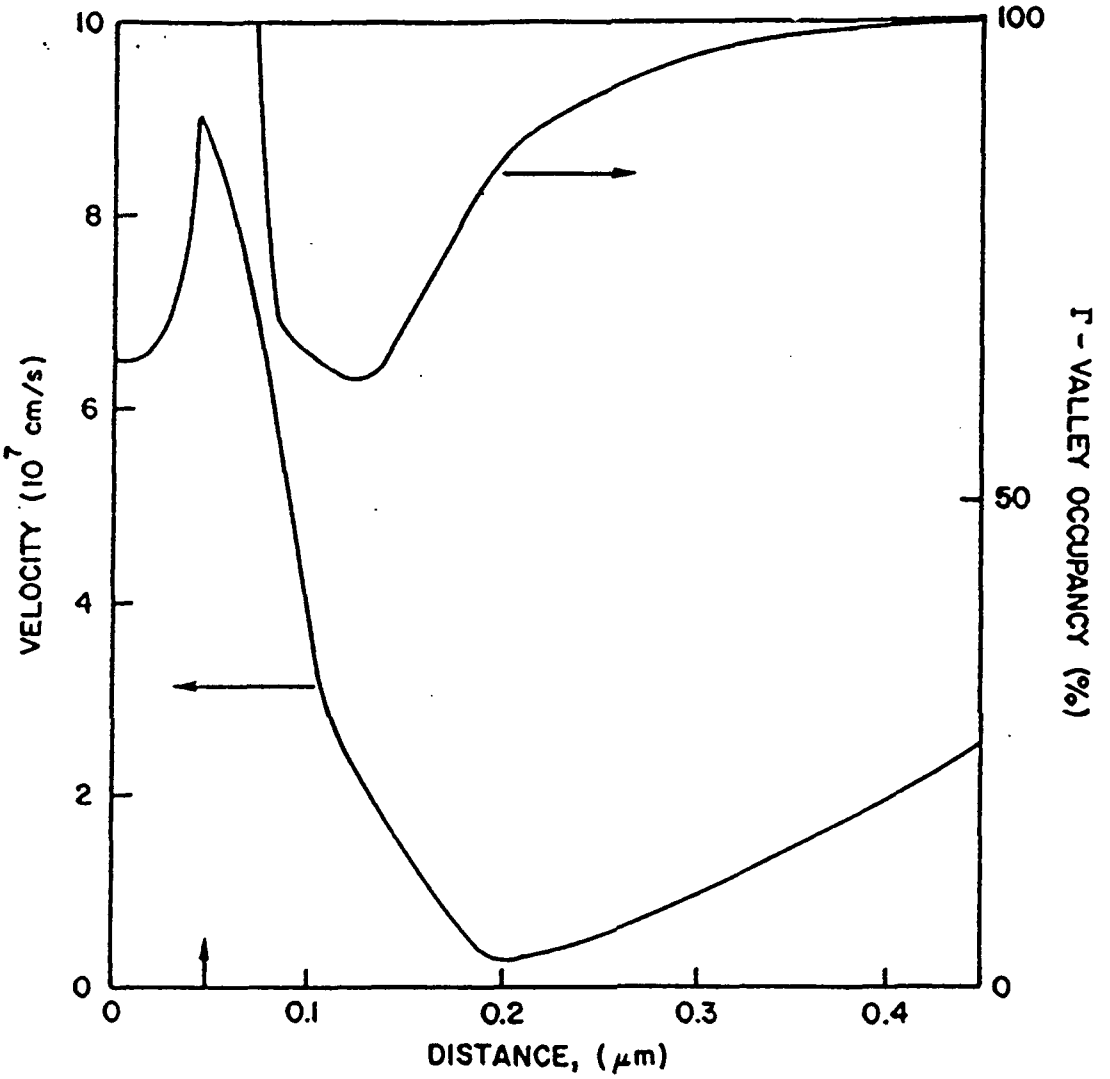

Figure 6. Plot of the Velocity and Central Valley Occupancy of the Electrons as a Function of Distance from Emitter Base Junction. The Base Width = 0.05 μm, $p^+ = 5 \times 10^{18}$ cm^{-3}.

MODELING OF LARGE SIGNAL DEVICE/CIRCUIT INTERACTIONS

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INTRODUCTION

The evaluation of the potential performance of semiconductor devices for analog applications is usually performed in two ways. First, the device may be characterized through small signal admittance or scattering parameters which may be obtained by experiment for existing devices or by numerical simulation for a new device structure prior to fabrication. From these results, the devices can be characterized in terms of small signal parameters such as the unity gain cutoff frequency, f_t, and f_{max}. While these parameters provide a valid estimation of the limits of the device operation under linear, small signal conditions, such estimate will typically be in error under large signal conditions. Under large signal, high power conditions, nonlinear effects within the device become important. At low frequency, the nonlinear effects manifest themselves primarily as bias dependent parameters such as bias dependent transconductance and capacitance. At high frequency these parameters will also exhibit hysteresis effects due to the nonequilibrium nature of transport within the device.

As a result of these nonlinearities it is imperative that the performance of the device be evaluated while embedded in its operational circuit. It is the device-circuit interaction and resulting performance that is of interest and not simply the device characterization. Since it is obviously too costly and time consuming to design, fabricate and test a new device and then design, test, and redesign a circuit around the device in hope of achieving the desired performance, an alternative must be found. This alternative is numerical modeling. Fundamentally, device-circuit interaction can be modeled using, for example, the drift and diffusion equations to represent the device and coupling the external circuit to it through boundary conditions. While this has been and will continue to be done, it is presently too costly, even on the supercomputers available today, for all but the simplest of circuits. As a result, devices are approximated by nonlinear equivalent circuit elements in the large circuit simulation procedures. The adequacy of these equivalent circuit models has a direct impact on the predicted results.

In an effort to improve these device models Madjar and Rosenbaum [1] and Khatibzadeh and Trew [2] have developed procedures in which the FET is modeled by a system of nonlinear ordinary differential equations relating the gate and drain currents to the time dependent gate and drain voltages. The coefficients of these ODE's are determined **analytically**, using highly approximate models of the device. The present work is a significant generalization of the approach of [1] and [2]. Here the coefficients of the ODE's representing the device are determined **numerically**, through a physically based model; in this case the drift and diffusion equations. The resulting ODE representation is then executed, and the validity of the results are verified, at select bias points, by performing transient accurate drift and diffusion simulations for steady AC operation. With such an

agreement established, the equivalent circuit model can then be used with a higher degree of confidence in a complex circuit simulation. While the drift and diffusion equations are used in the present work, the concepts are general and simulations based on nonequilibrium transport models (moments of the Boltzmann equation or Monte Carlo) could be substituted as deemed necessary.

ANALYSIS

The importance of the device-ciruit interaction, as well as well as the limitation of a completely general approach is illustrated in the first few figures. In a recent study of the design of the permeable base transistor (PBT) for high power applications [3], the large signal AC characteristics of the device and circuit were obtained from one cell of an array of permeable base transistors connected to a resonant circuit, as shown schematially in figure 1. **It is this device plus circuit that is subject to large signal numerical simulations.**

In the PBT power simulations the device is represented by the semiconductor drift and diffusion equations for electrons and holes, as discussed below and in [4]. The external circuit is represented by linear elements. A typical calculation involves applying a sinusoidal voltage to the gate at a specified frequency and calculating the current through, and the voltag across the load. For example, for the circuit of figure 1, and an input signal of 40GHz, the output is a function of the natural frequency of the resonant circuit and the phase of the resonant circuit relative to the phase of the driving signal. In [3], the effects of the external circuit were systematically studied by changing the relative values of the circuit inductance, L, and capacitance C, subject to the constraint that the LC product was fixed, i.e., the natural frequency was unchanged. The results are illustrated in figure 2 as a lissajous of gate and drain voltages, along with the indicated power gain variations. (Lissajous are obtained by eliminating time between, e.g., $V_g(t)$ $V_d(t)$, etc.) The significance of this lissajous is both its connection to specific phase relationships between the input and output, as are needed for the ODE device representation; and its ability to emphasize critical device-circuit dependence.

The above procedure is an extremely valuable research tool. But it has little hope of having any major impact in the design of a system. This shortcoming arises because: (1) The algorithms for the time-dependent drift and diffusion equation, as applied to gallium arsenide can require computational times measured in minutes of CRAY XMP time per calculation. (2) The algorithms require workers that are experts in numerical procedures. (3) The circuit represented by figure 1 is too simple to be of practical use; mpre complicated input and output waveforms are required, as arise from a circuit of the type shown generically in figure 3.

To reduce the computational time associated with the device, nonlinear equivalent circuit element representations of the device have been taken by a number of workers, e.g., Madjar and Rosenbaum [1], and Khatibzadeh and Trew [2]. Following [1] and [2] the gate and drain currents may be related to the terminal voltages as:

$$I_g(t) = I_g(V_g,V_d) + C_{11}(V_g,V_d)\frac{\partial V_g}{\partial t} + C_{12}(V_g,V_d)\frac{\partial V_d}{\partial t} \qquad (1)$$

$$I_d(t) = I_d(V_g, V_d) + C_{21}(V_g, V_d)\frac{\partial V_g}{\partial t} + C_{22}(V_g, V_d)\frac{\partial V_d}{\partial t} \qquad (2)$$

Madjar and Rosenbaum [1] as well as Khatibzadeh and Trew [2], use the above equations; both ignore any gate dc conductance. Additionally Khatizbzadeh and Trew [2] introduce phase lags for the gate voltage, as discussed below. We must point out that representing the currents through the device as a set of time dependent ordinary differential equations is a significant approximation.

In [1] and [2] a highly simplified model of the device is introduced to allow the coefficients in eqs. [1 and 2] to be evaluated analytically. Because of the approximations used to produce analytical solutions, the modeled region of the device is a severe truncation of the actual device. For example, Madjar and Rosenbaum [1], Khatibzadeh and Trew [2] and Khatibzadeh [5], represent transport in a recessed gate FET, as shown in figure 4 by transport through the shaded region. In this case, under an assumption of zero gate current, Khatibzadeh and Trew [2] compute the dc drain current voltage characteristics from the analytical model; I_d is generally a nonlinear function of V_g and V_d. For the nonlinear capacitance coefficients, Madjar and Rosenbaum [1] as well as Khatibzadeh and Trew [2], also computed these analytically. In this case, following Khatibzadeh [5]:

$$I_g = \frac{dQ_g}{dt} = \frac{\partial Q_g}{\partial V_g}\frac{\partial V_g}{\partial t} + \frac{\partial Q_g}{\partial V_d}\frac{\partial V_d}{\partial t} \qquad (3)$$

where Q_g is computed analytically from Gauss's law. A similar expression is obtained for I_d, the drain current. Note: the coefficients of the time derivatives of the gate and drain voltages are the terms C_{11} and C_{12} in equation (1). In the discussion below Q_g, Q_d and the C coefficients **are obtained numerically through a full two-dimensional transient physically based device simulation.** A related, but pseudo-two dimensional approach has recently been followed by Crosnier, Gerard and Salmer [6], where the field is assumed to be purely normal to the gate contact in the gate depletion region and parallel to the gate surface in the conducting channel. Current flow is taken as one dimensional in the channel region with varying cross-section and charge.

Since nonuniformities in the field profiles within a device are expected at high bias levels, it is anticipated that the analytical approximations will fail under these conditions. Further the effect of process properties, such as the source and drain diffusions, as well as such important designs features such as a buried layer or a heterostructure interface are completely ignored. In other words using the analytical tools described above, a design engineer cannot confident specify a device, especially a new device where ad hoc corrections to the analysis are not known.

To overcome these difficulties, better approximations to the capacitance coefficient are required and means of verifying them are necessary. To address these goals we have implemented a two-dimensional transient and steady state drift and diffusion code [4]. The present two-dimensional physically based device analysis is based on the solution of the

drift and diffusion equations for electrons and holes in compound semiconductors. The governing drift and diffusion equations are the continuity equations for electrons and holes and Poisson's equation:

$$\frac{\partial N}{\partial t} = \nabla \cdot \left[-N\mu_n \nabla(\psi+\psi_n) + D_n \nabla N \right] + G - R \qquad (4)$$

$$\frac{\partial P}{\partial t} = \nabla \cdot \left[P\mu_p \nabla(\psi+\psi_p) + D_p \nabla P \right] + G - R \qquad (5)$$

$$\nabla \cdot \epsilon \nabla \psi = e(N - N_D - P + N_A) \qquad (6)$$

where N and P are the electron and hole concentrations, respectively, and e is the electron charge. The quantity within the square brackets represents the electron and hole currents densities, $-J_n/e$ and J_p/e, respectively, G represents generation, R recombination, ψ is the potential, ϵ the permittivity, and N_D and N_A are the concentrations of donors and acceptor ions, respectively. The terms ψ_n and ψ_p are introduced to account for variations in the conduction and valence band energy levels. Through ψ_n and ψ_p such effects as band gap narrowing and heterojunctions may be accounted for.

Within the context of equations (4) through (6) materials such as gallium arsenide are represented by field dependent mobilities with a region of negative differential conductivity (NDC). While NDC is included in the proposed program we point out that it is a feature never included in the analytical representations of nonlinear devices. Recently, Curtice [7] applied a two-dimensional electron temperature model to short gate devices, and developed both small and large signal equivalent circuit models for the GaAs FET.

The present study used the device shown in figure 5. This device is from Snowden et al [8]. The DC I-V characteristics of the device were computed using the drift and diffusion analysis. A mesh of 25 by 89 unequally spaced points was used. The computational mesh is shown in Figure 6a. The distribution of electron density and electric field are shown in Figures 6b and 6c for a DC operating point at V_g = -2 volts and V_d = 4 volts. For the present calculations the mobility model of [8], was used. The resulting I-V characteristics are presented in Figure 7 where the calculations of Snowden et al [8] and the experimental measurements are also presented. Using our drift and diffusion analysis breakdown was seen to occur between 5 and 6 volts on the drain, which is where the measurements stop.

These breakdown results demonstrate the importance of including as much physics as possible in the drift and diffusion calculations. Without a model of device breakdown the design engineer could mistakenly use calculated device characteristics that in some regions do not even approximately represent device operation as shown by the solid lines in Figure 7 at drain voltages above 5 volts. What is true, in this example, of the importance of including breakdown in the drift and diffusion simulation is also true of other physical phenomena such as accurately representing the doping variations within the device, accurately representing the substrate and its effects on the performance of the device,

computing surface states and thermal effects and the effects of traps. Each of these phenomena can be important in different regions of device operation. For accurate modeling of a device the phenomena that are important in the region of operation must be incorporated in the drift and diffusion calculation as accurately as possible.

After computing the DC I-V characteristics, a least-squares bivariant polynomial curve fit was performed for the drain and gate currents and charges as a function of gate and drain voltage. Note; the charge on each contact is given by the change in the displacement relative to a reference bias point. After curve fitting the capacitive coefficients are obtained analytically from

$$C_{ij} = \frac{\partial Q_i}{\partial V_j} \tag{7}$$

To utilize the above DC characteristics to compute AC device operation, phase delays were introduced into equations 5 and 6. Katibzadeh, [5], used a phase delay of the form:

$$C_{ij}(V_g(t),\ V_d(t)) = C_{ij}(V_g(t-\tau), V_d(t)) \tag{8}$$

In the present study three phase delays are introduced into the analysis. Two of these (τ_1, τ_2) correspond to readily observed phenomena. The third, τ_3, was introduced because of symmetry in the equations but its value was set to zero since, in the case studied, it was part of a term that was one to two orders of magnitude smaller than adjacent terms and could not be determined. As used in this study, the equivalent circuit equations for the AC operation of the FET of figure 5 is:

$$\begin{aligned} I_g = I_g^o &+ C_{gg}(V_g(t), V_d(t-\tau_1))\frac{\partial V_g}{\partial t}(t-\tau_2) \\ &+ C_{gd}(V_g(t), V_d(t-\tau_1))\frac{\partial V_d}{\partial t}(t) \end{aligned} \tag{9a}$$

$$\begin{aligned} I_d = I_d^o &+ C_{dg}(V_g(t-\tau_1), V_d(t))\frac{\partial V_g}{\partial t}(t) \\ &+ C_{dd}(V_g(t-\tau_1), V_d(t))\frac{\partial V_d}{\partial t}(t-\tau_3) \end{aligned} \tag{9b}$$

where I_g^o is the DC gate current and I_d^o is the DC drain current.

The phase delays τ represent cycle averaged responses of the device to AC inputs. In steady AC operation the phase delay τ_1 controls the slope of the major axis of the V_g-V_d lissajous and τ_2 controls the slope of the major axis of the I_g-V_g lissajous. Single values of τ_1 and τ_2 were computed from power calculations with a resistive load on the drain at 20, 40 and 60 GHz to minimize the discrepancy in computed power between equations 12 and the drift and diffusion calculation at those frequencies.

Although the influence of τ_1 and τ_2 on the lissajous is known, these parameters may each represent the effects of several physical phenomena within the device. In particular τ_1 may represent a transit time for charge pulses to move from gate to drain, plus the response time of the depletion region under the gate as it becomes a source or sink for charge as the gate voltage is changed. The phase delays used in equations 9 are also functions of the magnitude of the imposed signal, the frequency and the DC operating point. These dependencies have not fully been established. Understanding the physics of phase delays will permit accurate use of this nonlinear equivalent circuit model over a broad range of operating conditions.

RESULTS

The above equivalent circuit model was compared to the drift and diffusion calculation of the FET of figure 5 in AC operation at 20, 40 and 60 GHz with a resistive load on the drain. Lissajous of these calculations are presented in figures 8 and 9. Comparisons of three power gain calculations at the same frequencies are shown in table 2. The lissajous, after the initial transient, and the AC power calculations are well represented by the equivalent circuit analysis.

To demonstrate the utility of the equivalent circuit model an optimization program was mated to the **equivalent** circuit model. The optimization program drove the gate and drain voltages sinusoidally with an imposed phase delay:

$$V_g = V_g^o + \Delta V_g \sin(\omega t) \qquad (10a)$$

$$V_d = V_d^o + \Delta V_d \sin(\omega t - \phi) \qquad (10b)$$

The following optimization problem was posed: For fixed V_g^o = -2 volts, V_d^o = 4 volts and ΔV_d = 1 volt what values of ΔV_g and ϕ will provide a power gain of 8 db at an input power of 10^{-2} watts. ΔV_g was constrained to be in the range $0 \le \Delta V_g \le 1.5$ volts. This problem was solved at a series of frequencies from 10 GHz to 50 GHz. For frequencies from 10 to 20 GHz the desired power gain of 8 db was achieved. Above 20 GHz the power gain decreased as a function of frequency as shown in figure 10. Solution of the above problem at each frequency required 30 to 90 AC device calculations. This would be unreasonably time consuming and expensive for a drift and diffusion analysis even on modern supercomputers. Using the equivalent circuit model each optimization requiring 30-90 AC steady state device calculations took approximately 1 minute of time on an IBM PC AT or Macintosh Plus personal computer.

CONCLUSIONS

The present study demonstrates the feasibility of using a physically based research algorithm to generate the coefficients for a nonlinear, equivalent circuit model of an FET. The comparison of results computed using both the drift and diffusion equations and the equivalent circuit model for AC operation into a simple resistive load give some degree of confidence in the equivalent circuit model.

However, it is stressed that the equivalent circuit results must always be regarded as preliminary. It is always necessary to selectively verify them against physical models; and against experiments.

ACKNOWLEDGEMENTS

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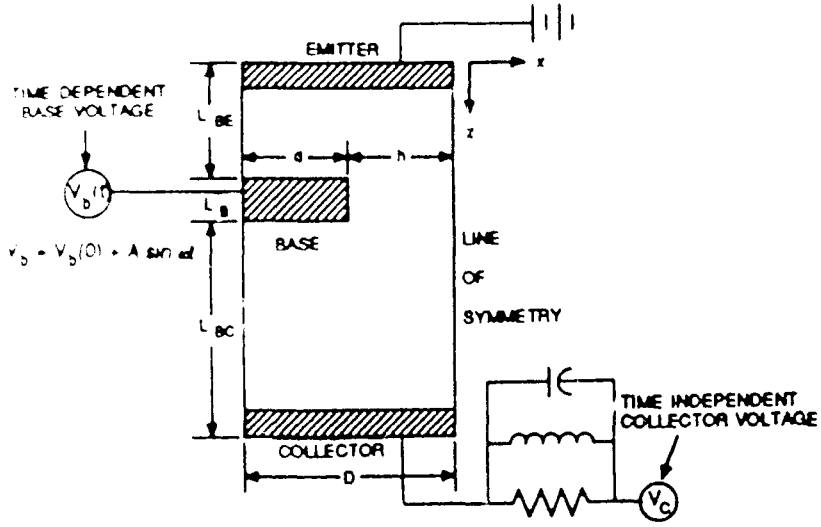

Figure 1. Large Signal PBT/Circuit Configuration.

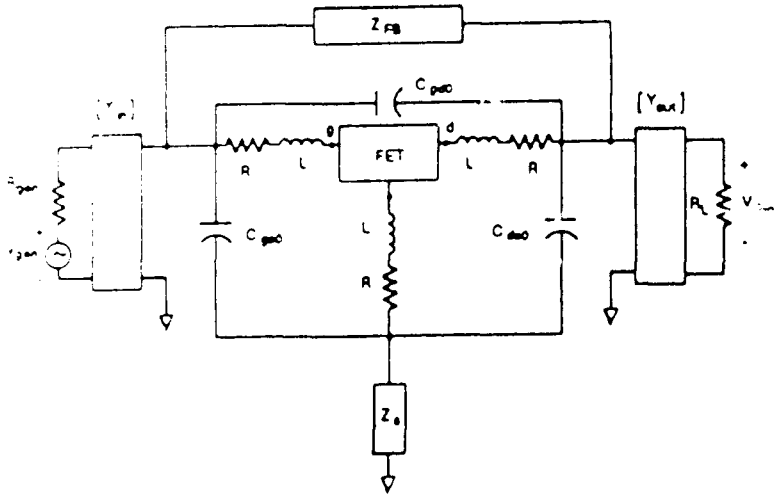

Figure 3. Topology of a single-FET Circuit.

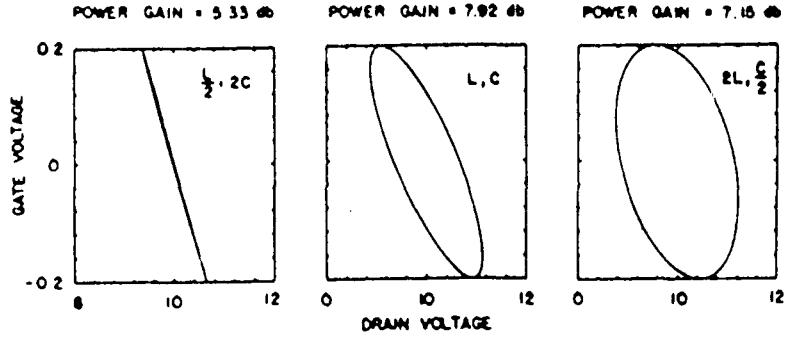

Figure 2. V_g vs. V_d Lissajous for a natural circuit frequency of 80 GHz. Input gate frequency is 40 GHz.

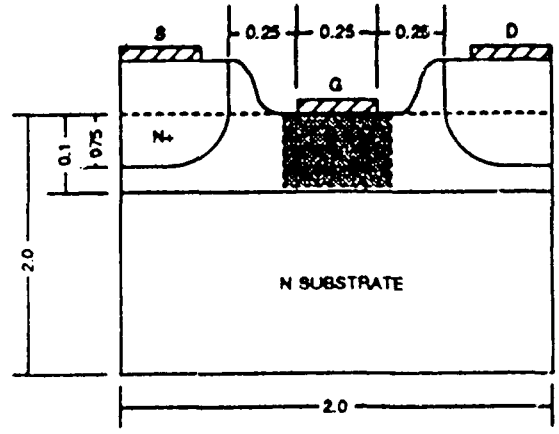

Figure 4. Schematic representation of FET Structure to be used in Phase I study. The recessed gate will not be considered under Phase I. N^+ region doped to $1x10^{18}/cm^3$, N region to $1x10^{17}/cm^3$, substrate is semi-insulating GaAs. The shaded region represents that portion typically studied analytically.

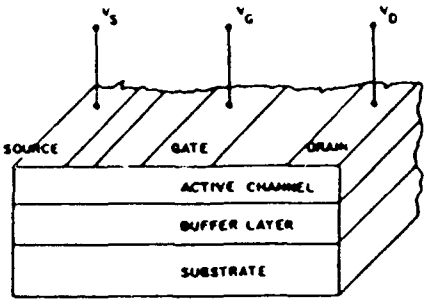

Figure 5. FET Schematic from Ref.8.

GATE LENGTH	0.55 μm
GATE WIDTH	300 μm
CHANNEL THICKNESS	0.15 μm
SOURCE TO GATE SPACING	0.5 μm
DRAIN TO GATE SPACING	0.6 μm
BUFFER LAYER THICKNESS	0.2 μm
GATE METALLIZATION	ALUMINUM
SCHOTTKY BARRIER HEIGHT	0.80 V
TEMPERATURE	350 K
DOPING OF ACTIVE LAYER	1.5×10^{23} m^{-3}
DOPING AT CONTACTS	3.7×10^{23} m^{-3}
SUBSTRATE IMPURITY LEVEL	1.0×10^{23} m^{-3}

Table 1. Physical parameters for the 0.5 μm Gate Length GaAs MESFET used in the Simulation.

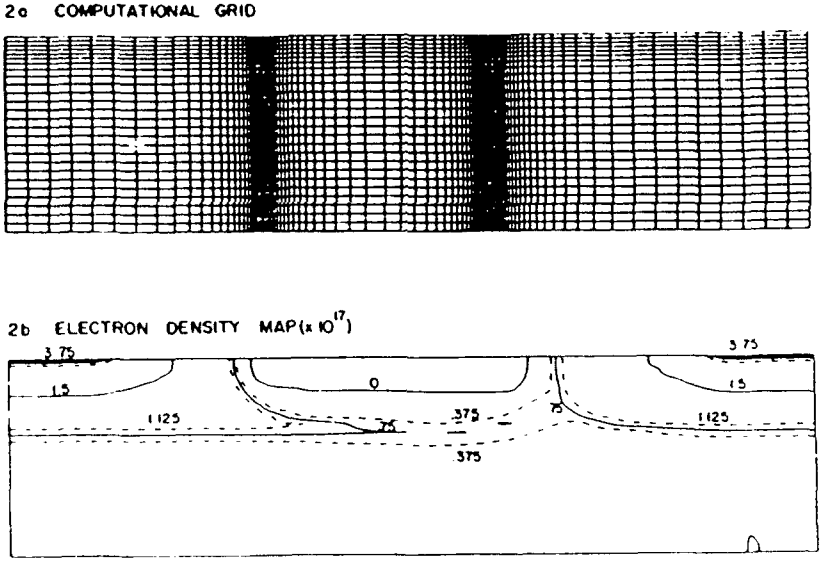

Figure 6. Two-Dimensional Device Simulation.

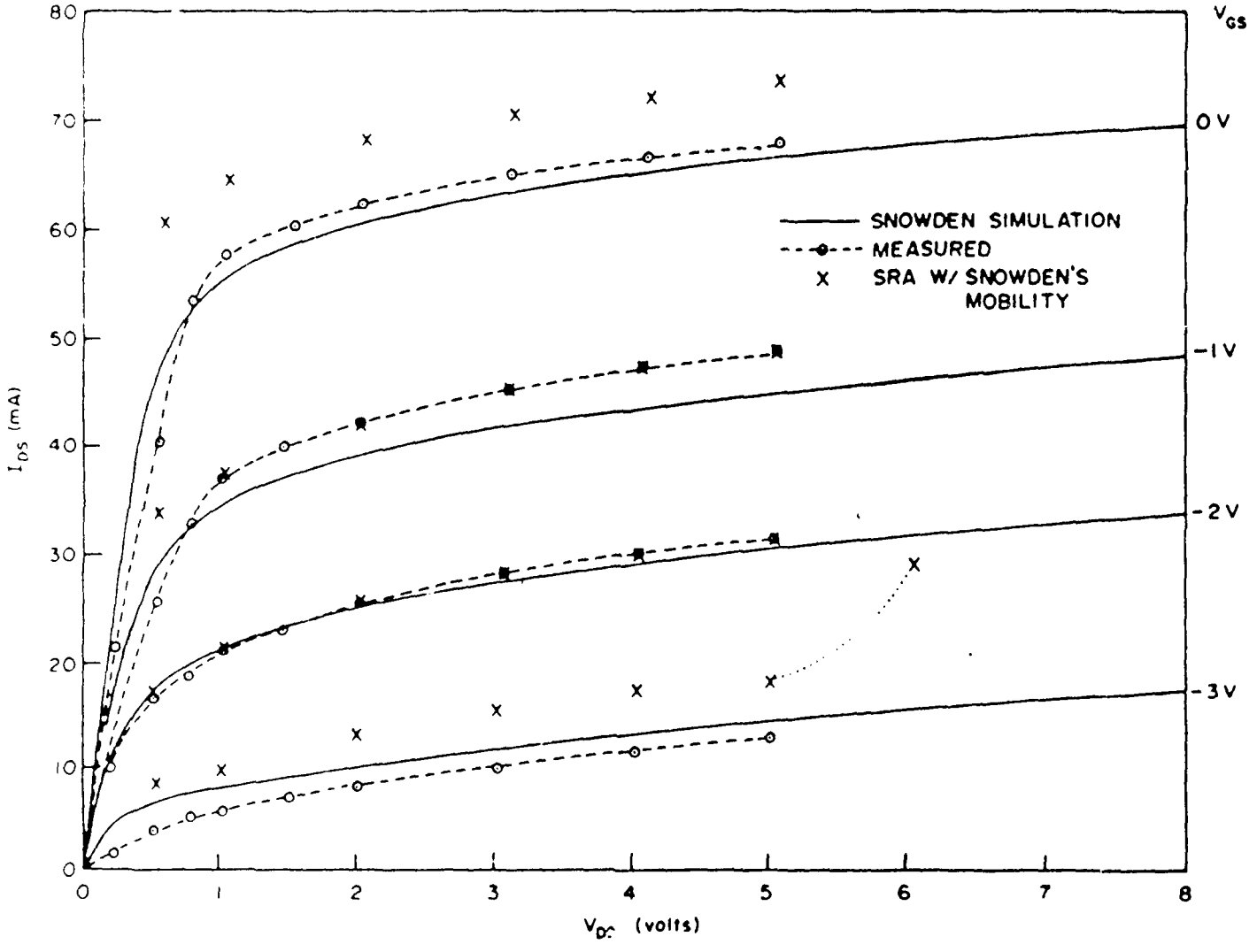

Figure 7. I-V Characteristics of a FET - Measured and Computed.

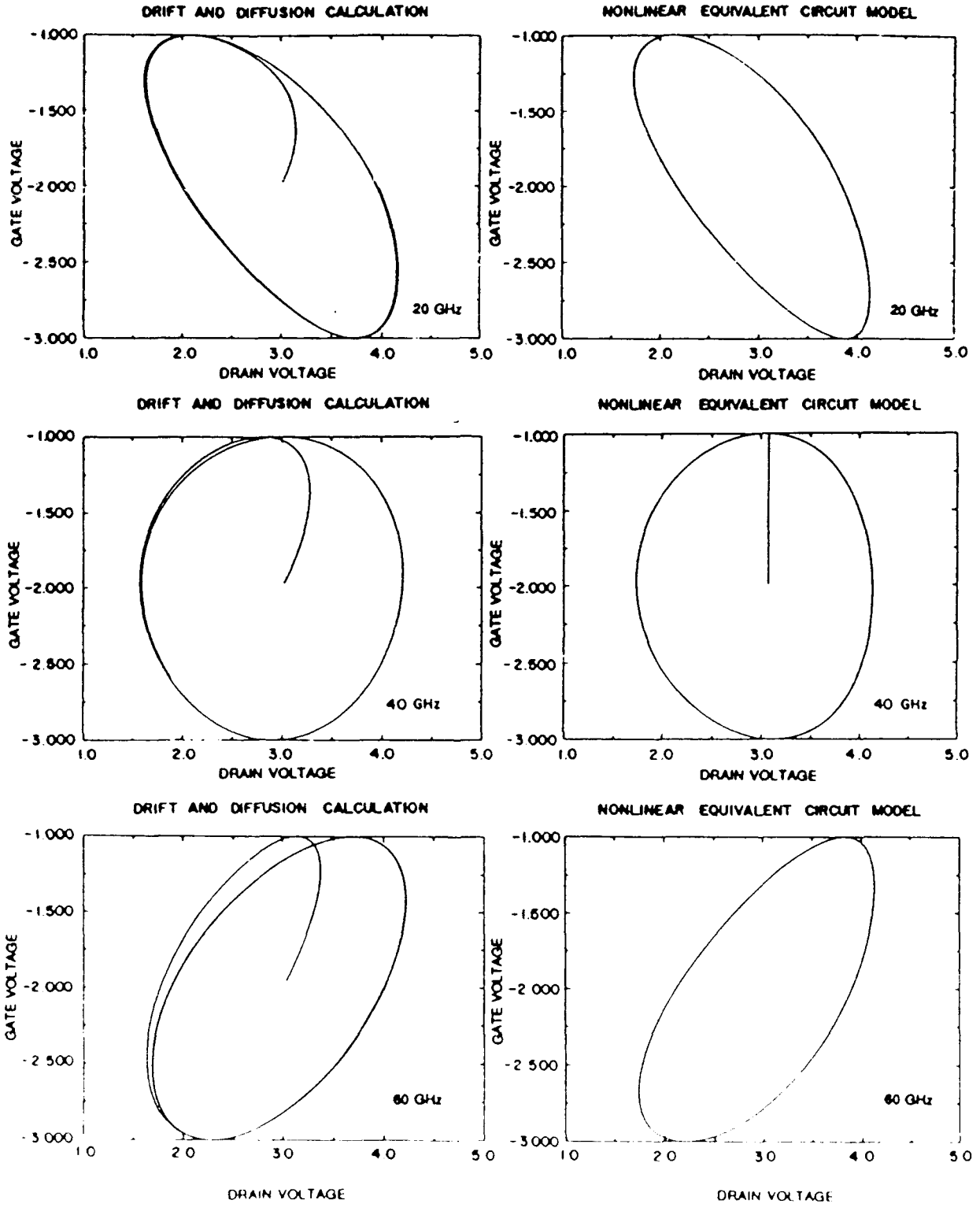

Figure 8. V_g-V_d Lissajous Comparison.

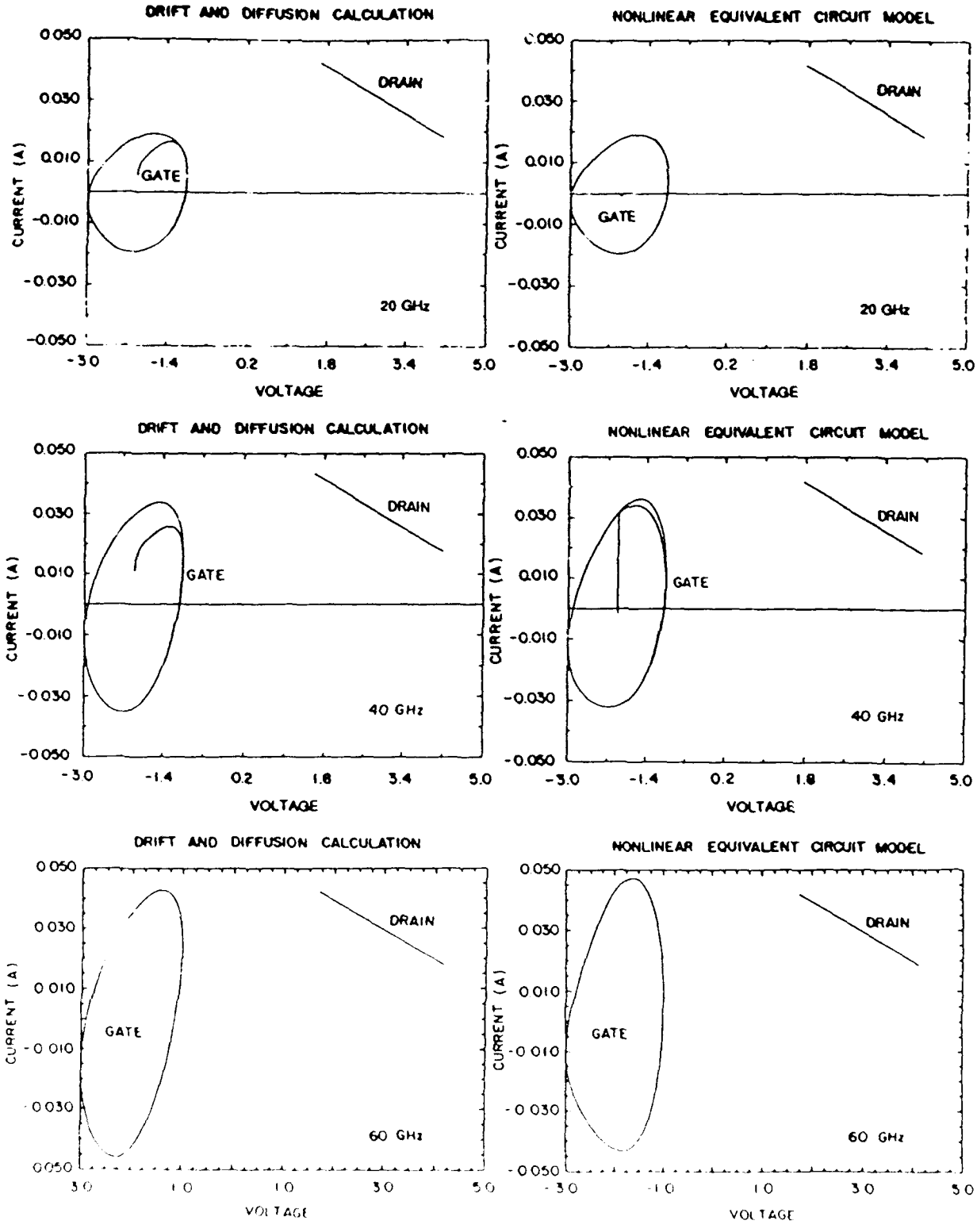

Figure 9. I-V Lissajous Comparison.

	DRIFT AND DIFFUSION CALCULATION	NONLINEAR EQUIVALENT CIRCUIT MODEL
20 GHz	3.92	4.03
40 GHz	1.32	1.25
60 GHz	0.78	0.80

Table 2. Ratio of Output Power to Input Power - Comparison of Drift and Diffusion Calculation and Nonlinear Equivalent Circuit.

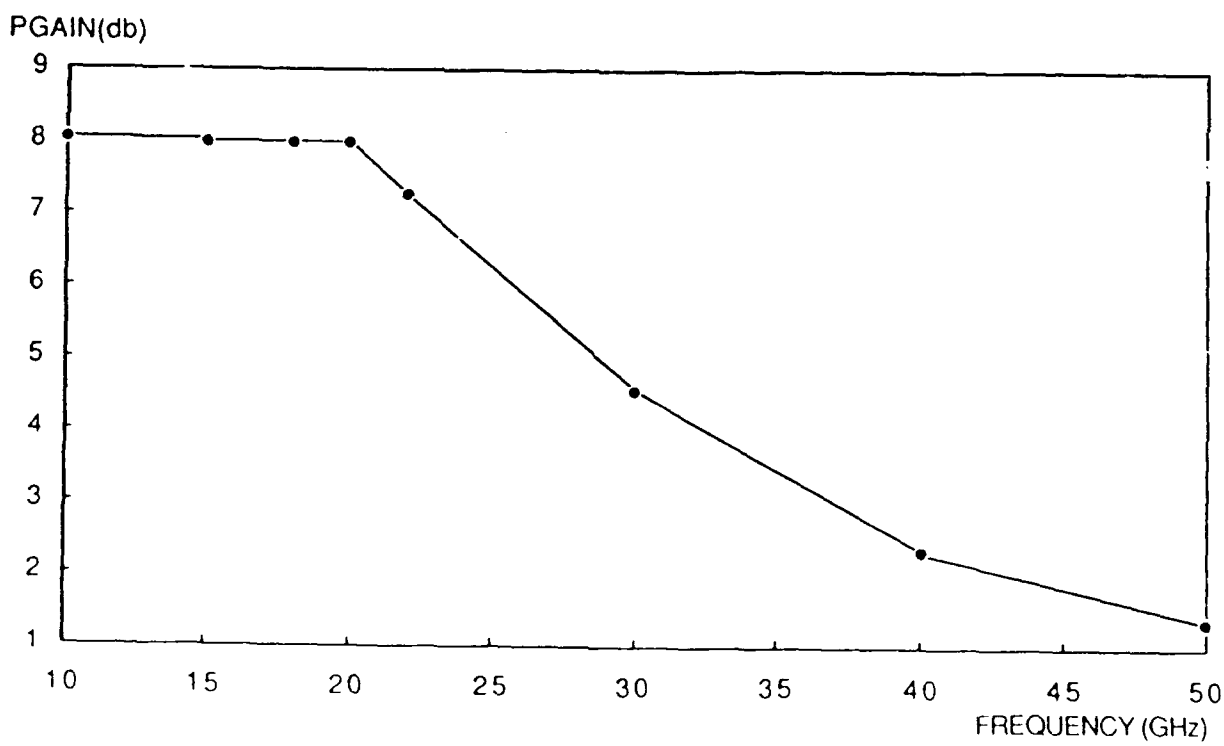

Figure 10. AC Power Gain vs. Frequency at Fixed Input AC Power.

To be submitted for publication.

LARGE SIGNAL, DRIFT AND DIFFUSION EQUATION POWER CALCULATIONS FOR FIELD EFFECT TRANSISTORS

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I. INTRODUCTION

The evaluation of the potential performance of semiconductor devices for analog applications has heretofore been approached through two distinct processes: (i) small signal characterization as obtained from admittance or scattering calculations [1], or (ii) large signal ordinary differential equation (ODE) representations of devices coupled to their respective linear circuits [2]. In some cases further advances involve coupling the ODE representation of the device to a complex embedded multiple element array. While these descriptions are direct they are extremely limited in their predictive abilities because they do not adequately represent such key features as the transient charge distribution within devices, and do not, thereby permit design engineers to introduce changes in the structure of the transistor to minimize the consequences of uncontrolled process variations. What is required, as is discussed below, is a physics based approach that couples the equations governing transport within the device to those equations that represent the external circuit. The results of such an approach should enable designers to isolate the dependence of the results upon two features, the design of the device, e.g. contact placement, doping profiles, position of the interface layers, etc., and the structure of the external circuit. An algorithm has been developed that incorporates the necessary device circuit coupling and identifies the interdependence of the semiconductor device properties and the circuit and the nonlinear transients (SECANT). The algorithm has been successfully applied to studying the analog performance of field effect transistors. The first application for SECANT has been the gallium arsenide permeable base transistor (PBT) [1]. This paper very briefly describes the salient features of SECANT.

The essence of the approach is represented by Figure 1, which shows a two dimensional representation of a PBT connected to an external reactive element circuit. (Note that FET terminology, rather than PBT terminology is used in this paper.) Transport in the semiconductor is represented by the spatial and temporal dependent drift and diffusion equations for gallium arsenide. The circuit is represented by ordinary differential equations. Both device and circuit equations are solved simultaneously. While the purpose of this paper is to illustrate the significance of performing large signal physically based power calculations, the results, as they relate to the PBT are significant. In particular, it is concluded that the achievement of power in excess of 3/4 watt at 40 GHz is a distinct possibility for the PBT.

The discussion is divided into several parts. The structure of the calculation and the results are discussed in sections II and III, respectively. Section IV contains the broad conclusions of the analysis.

II. STRUCTURE OF THE CALCULATION

In the following the large signal operation of the transistor is obtained from solutions to the semiconductor drift and diffusion equations. Carrier ionization and hole transport are ignored in the transient calculation, although time independent dc calculations at one value of gate voltage include both, are carried to breakdown, and are included in the study. The semiconductor drift and diffusion equations for electrons include the continuity and Poisson equations, respectively:

$$\frac{\partial N}{\partial T} - \frac{\nabla \cdot J}{q} = 0,$$

$$\nabla^2 \Psi - (q/\epsilon)(N - N_D) = 0$$

Here N,J [$= q(-N\mu\nabla\Psi + D\nabla N)$] and Ψ are the carrier density, current density, and the potential, respectively. N_D is the background doping, q is the electron charge, μ and D are the field-dependent electron mobility and diffusivity, and ϵ is the permittivity.

For gallium arsenide the field dependent mobility is obtained from the field dependent drift velocity, the latter being shown in figure 2 for different doping levels. The diffusivity is field dependent and obtained from the Einstein relation. Typical time independent boundary conditions are discussed in [3]. Under time dependent conditions these are modified as follows: For the gate contact:

$$V_g(t) = V_g(0) + V_g \sin 2\pi f t$$

where $V_g(0)$ is the quiescent bias or dc point, V_g is the amplitude of the imposed sinusoidal gate voltage, and f is the imposed frequency. For the drain contact the time dependent boundary condition is obtained from the governing reactive circuit equations. The choice of the inductance L and the capacitance C for the reactive circuit is constrained by the condition:

$$f_r = 1/2\pi [LC]^{\frac{1}{2}}$$

In many of these calculations discussed below f_r is fixed while the values of L and C,are varied. In each of these calculations one combination of L and C is such that $1/RC = 2\pi f_r$. Hence changes in the values of L and C result in changes in both the Q and phase of the circuit. But it must be noted that the response of the carriers in the device are not necessarily linear, and the resulting device circuit interaction is not necessarily that expected from linear circuits. However, as expected the phase of the reactive circuit, has a profound effect on the gain of the device; and maximum gain occurs for circuit frequencies, f_r, significantly different from the imposed gate frequency, f.

III. RESULTS

Figure 3 displays select dc characteristics of the PBT for the structure shown in Figure 1. The calculation at 0.4 volts is the only one to include both electrons and holes and is carried to breakdown. The breakdown voltage defines the limit of device operation for this study, although the power calculations performed below are for electrons only and ignore breakdown. In all of the calculations reported below the the load is time dependent. Preliminary calculations, not reported below, were performed for a static resistive load. For these calculations the drain resistance was chosen so that at zero drain current the drain voltage was 20 volts, and at zero drain voltage the dc current was 0.3 amps/cm. The same value of resistance was chosen for the dynamic load. Note: under steady state time independent boundary conditions and a purely resistive load, dc operating points are defined by the intersection of the dc load line with the dc IV curves.

The transient terminal characteristics were obtained for a wide range of bias conditions and frequency combinations. Of interest, of course, are calculations in which the circuit and driving frequencies are the same. These are discussed below. But to emphasize the potential of the calculation initial illustrations are for those cases in which the circuit and driving frequencies are different.

The time dependent terminal characteristics, when a sinusoidal voltage is applied to the gate of the PBT is shown in figure 4 (the current is in multiples of 2.4 amps/cm) for a full PBT cell for a gate voltage of amplitude 1.0 volts, centered about a dc operating point of -0.6 volts, an imposed gate frequency of 40GHz and a circuit frequency of 60 GHz. Note that the initial transient is followed by steady state periodic 40 GHz oscillation. The terminal characteristics are a consequence of simultaneous solutions to the drift and diffusion equations and the external circuit and reflect the transient charge distribution within the transistor, as illustrated in figures 5. Figure 5 displays density and potential contours at two instants of time and at the same approximate value of gate voltage; where in one case the gate voltage is increasing, and in the second the gate voltage is decreasing. Note the differences in the contours. These differences arise solely from the dynamic nature of the charge distribution at these frequencies. (In these figures, the source and gate contacts are at the bottom and left of the structure, respectively. Voltage contours are in multiples of volts, density contours are in multiples of $5 \times 10^{16}/cm^3$.) Included in figure 5 is a lissajous figure of the gate and drain voltage, obtained by eliminating time from the transient calculations displayed in figure 4. (Additional lissajous are displayed in figure 6.) We note that in a resistive circuit, calculations performed by the authors also display lissajous behavior of the type shown in figure 5. At low or dc frequencies the gate drain lissajous should degenerate to a straight line.

The gate drain voltage lissajous for different combinations of L and C, with the circuit frequency constrained to 60 GHz, is displayed in figure 6.. Note that there is clearly an increase in the area within the curve and that the minimum and maximum voltage levels are altered. In addition, if these closed curves are viewed as approximations to ellipses, then there is an apparent shift in the slope of the major axis. Reading from left to right in the figure, the gains are respectively, 7.1, 6.2 and 5.7db .

We digress for a moment and point out in performing the power calculations, several steps are taken. First the relevant current and voltages are Fourier analyzed. Then time averages of the input power, $< I_g(t)V_g(t) >$, and the output power $< I_d(t)V_d(t) >$, are computed. The gain is the ratio of the ac output power at a particular frequency to the input power at that frequency. In the calculations discussed below, while there was some harmonic contribution, virtually all of the power is confined to the fundamental, and this is the power and gain that is reported.

In addition to the lissajous of gate-drain voltage, the gate and drain current-voltage lissajous were also computed. This is displayed in figure 7. The gate current-voltage lissajous is displayed in the left hand part of each frame, while the drain current-voltage lissajous is displayed in the right hand part of the frame. Please note that the looping in the drain current-voltage lissajous is a consequence of differences between the drive and circuit frequencies. For the situation when the circuit and drive frequencies are equal the lissajous degenerates to a straight line.

Figures 8 through 11 display results for a circuit frequency that is tuned to twice the drive frequency. Figures 8 and 9 are for a driving amplitude of 1.0 volt, while that of figures 10 and 11 are for a driving amplitude of 0.6 volts. As seen in these figures the structure of the oscillation is ostensibly more complex, indeed there is some increase in harmonic content, but the general character of the oscillation is unchanged. With respect to figure 8, reading from left to right, the gains are, 4.0, 6.7 and 7.0 db, respectively. With respect to figure 10, the gains and, 4.0, 6.6 a,d 6.9, respectively.

Additional calculations were performed at driving frequencies equal to the circuit frequencies. For these calculation it was anticipated that the results would not depend on the relative values of the circuit inductance and capacitance. Calculations were performed to check this and they were verified. Figure 12 displays the gate drain voltage lissajous for different driving amplitudes. Note that the slope of the lissajous is different from that of the earlier figures where the driving frequency was below that of the circuit frequency. The gain for each of these calculations, within the numerical accuracy of the calculations was approximately 4.8 db, independent of input power.

The calculations reveal that the slope of the gate drain voltage lissajous is dependent upon the relative values of the circuit and drive frequency. This is apparent from a comparison of figures 6, 8 and 12. It is further emphasized in figure 13 where the circuit frequency varies from 20 GHz to 80 GHz. Note the gradual shift of the major axis. For these calculations in order of increasing circuit frequency, the gain is 1.6, 5.3, 6.5, and 5.3dB, respectively.

The situation at lower drive frequencies was also investigated, and are displayed in figure 14 for a driving frequency of 20 GHz. These calculations reveal the expected much higher gain. Note also the slope of these curves. In order of increasing circuit frequency the gains were respectively, 11.5 and 15.0 dB.

The gain studies are summarized in figure 15 for an array of 150 identical PBT cells and a depth of 25 microns. Note that the lower the frequency of oscillation, the higher the gain. Second, for a given signal frequency on the gate, the gain is dependent upon the phase of the circuit, all with the exception of a circuit tuned for the driving signal. It is clear that the calculations at this point have not yielded any compression,; higher drive is needed for this to occur. In addition these calculations suggest that for the repetitive structure considered here that an an output power of approximately 70 mw at 40 GHz is a distinct possibility.

IV. CONCLUSIONS AND RECOMMENDATIONS

The results of the study indicate that large signal device circuit interaction can be studied effectively through solution to the semiconductor drift and diffusion equations coupled to the circuit equations. The dependence of the result on the phase of the circuit is a new feature to be explored. With respect to the PBT the results of the study indicate that at least at frequencies near 40 Ghz, the PBT is capable of providing gain under large signal conditions. With gains as high as 7db at small signal operation, it is very likely that

respectable gains can be achieved at 60 and 94 GHz.

Each of the above results is dependent upon the circuit parameters. One parameter that was not varied in these calculations was the load. In a situation that mimics conditions normally applicable to small signal calculations where the drain voltage does not vary upon application of a change in gate voltage, similar calculations were performed. These calculations do not show any gain at 40 GHz.

The calculations discussed here demonstrate the possibility of 70 mw of power at 40 GHz for an array of 150 identical PBT cells and a depth of 25 microns. If the performance can be maintained by increasing the doping level to $2 \times 10^{17}/cm^3$, then a factor of four increase in output power can be achieved. If further, the device width of 25 microns can be tripled, then outputs of the order of 800 mw or better are possible.

ACKNOWLEDGEMENT

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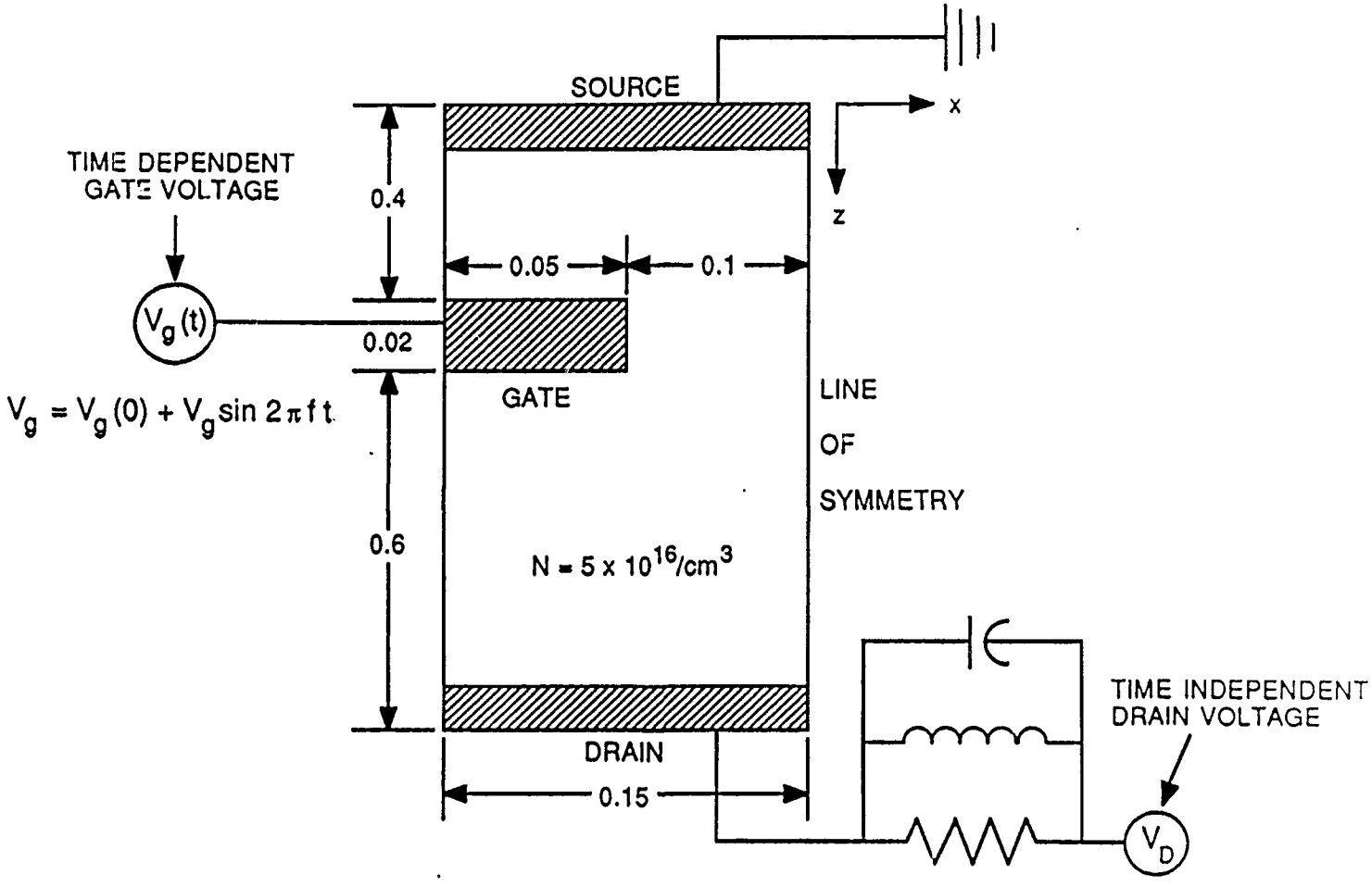

Figure 1. Large Signal PBT - Circuit Configuration
Time Dependent Gate and Drain Perturbation.

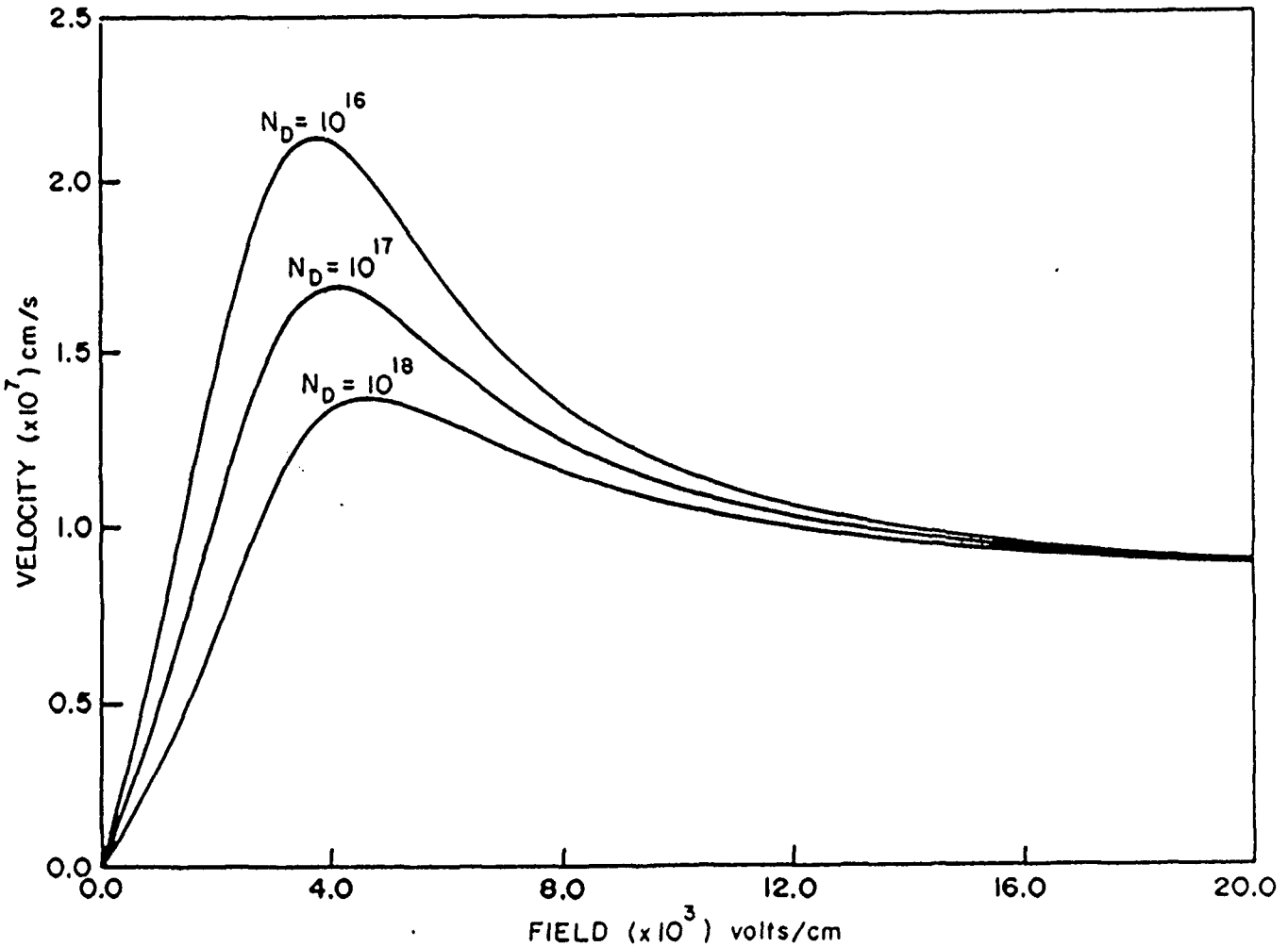

Figure 2. Velocity-Field Curve for GaAs.

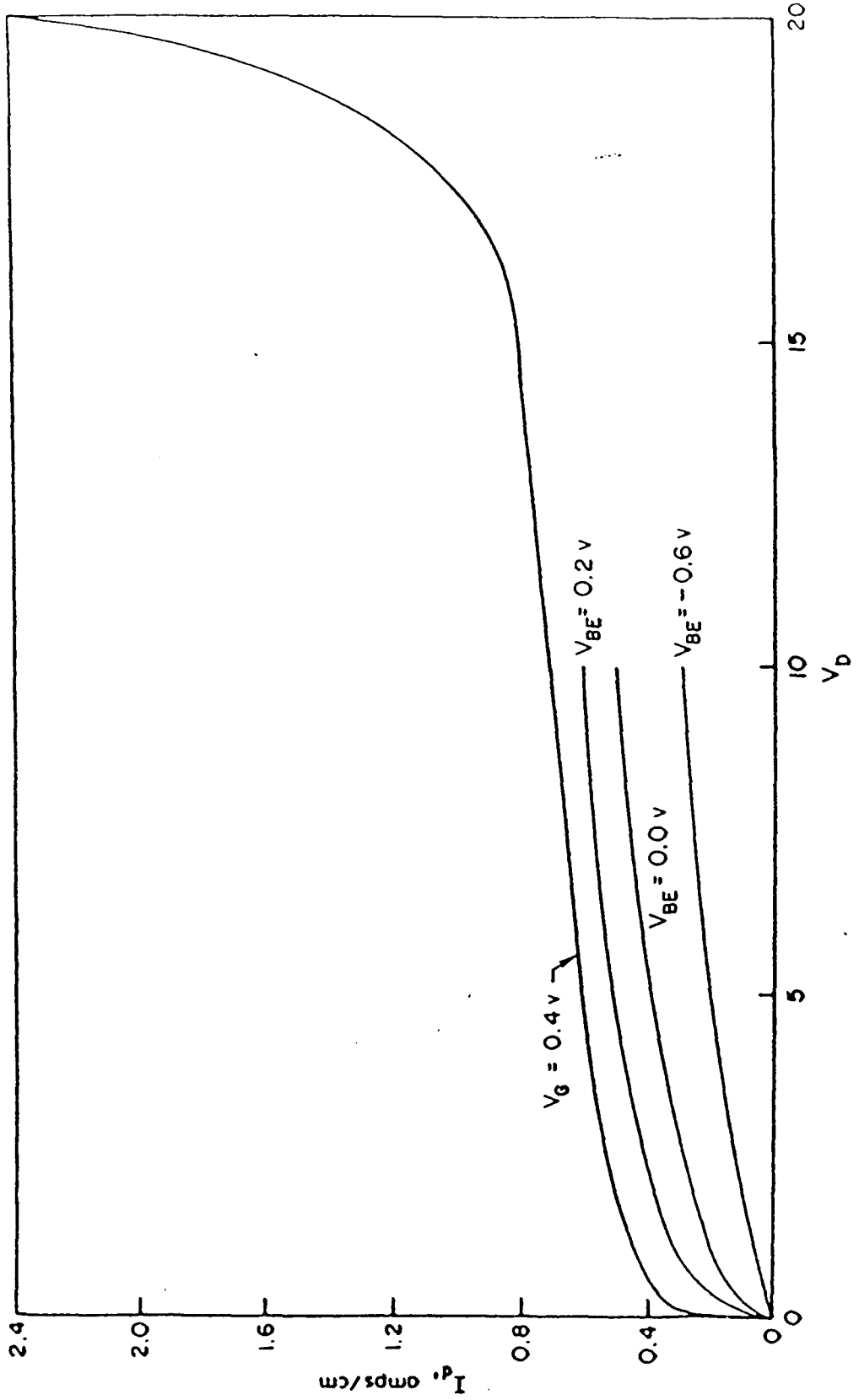

Figure 3. Select DC Characteristics - Breakdown Curve.

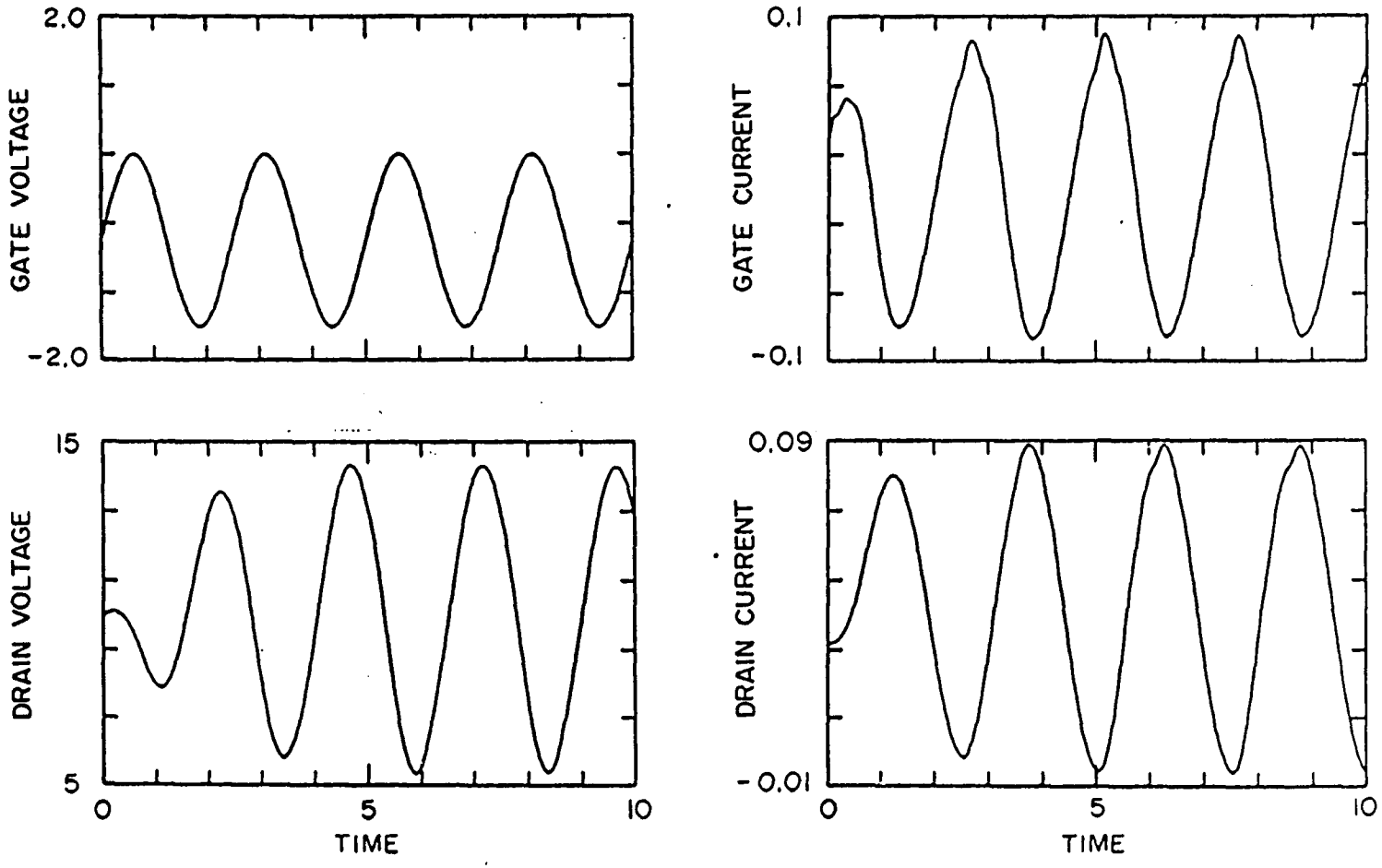

Figure 4. Time Dependent Current and Voltage through Gate and Drain for $V_g(0) = -0.6$, $V_g = 1.0$, $f_r = 60$ GHz, $f = 40$ GHz, $C = 5.10 \times 10^{-16}$ farad, and $L = 1.38 \times 10^{-8}$ henry.

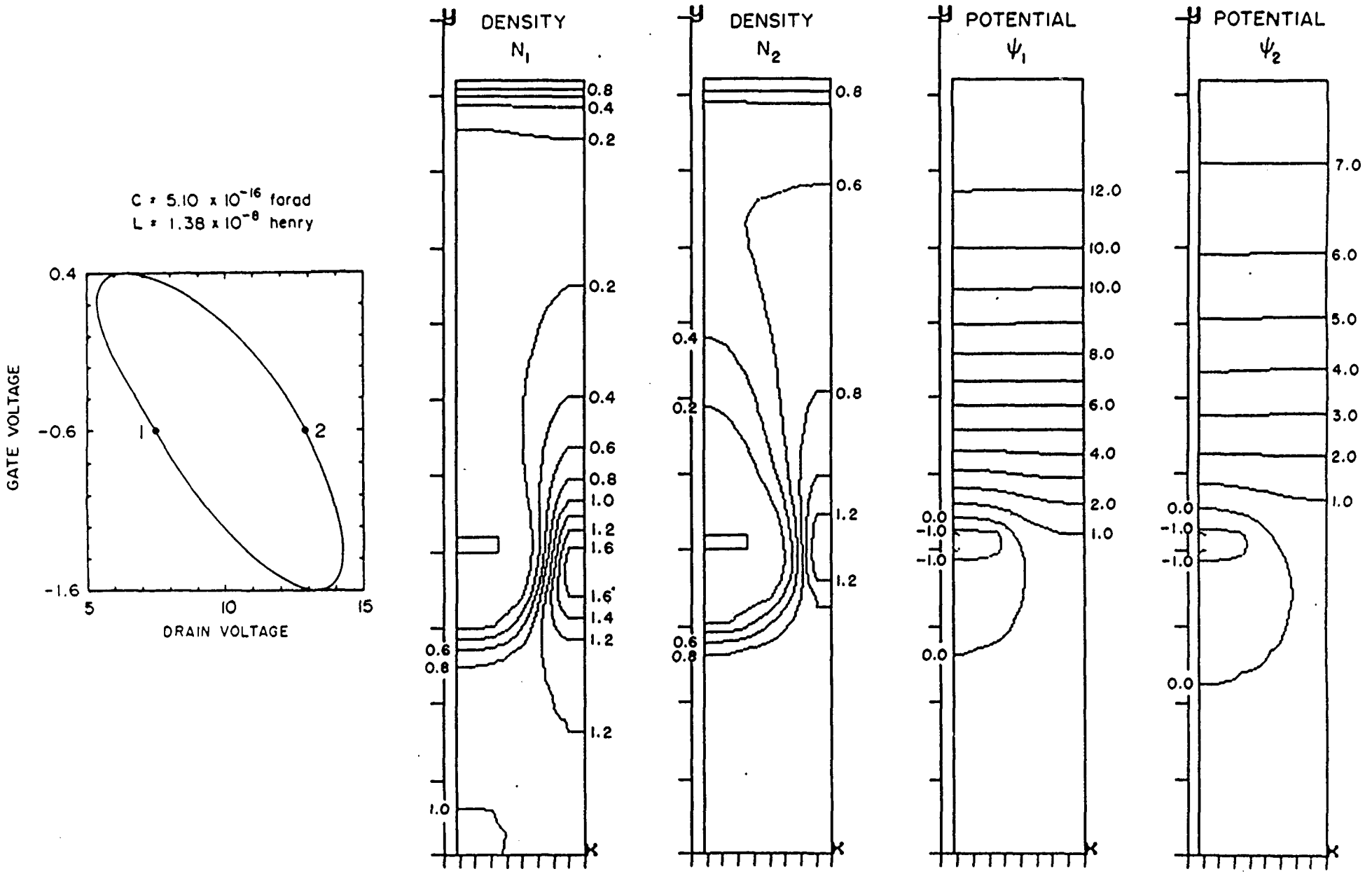

Figure 5. Density and Potential Contours for $V_g(0) = -0.6$, $V_g = 1.0$, $f_r = 60$ GHz, and $f = 40$ GHz.

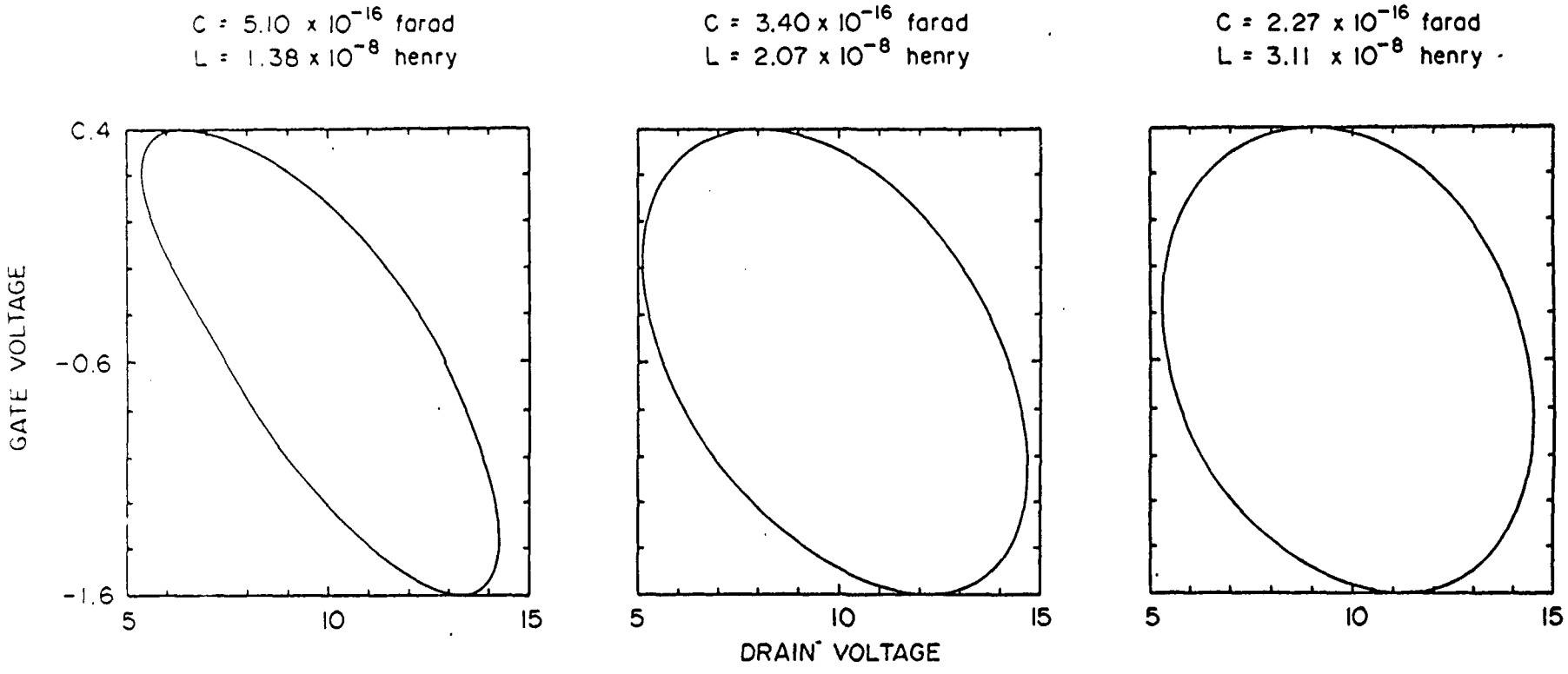

Figure 6. Gate Drain Voltage Lissajous for $V_g(0) = -0.6$, $V_g = 1.0$, $f_r = 60$ GHz, $f = 40$ GHz and different combinations of inductance and capacitance.

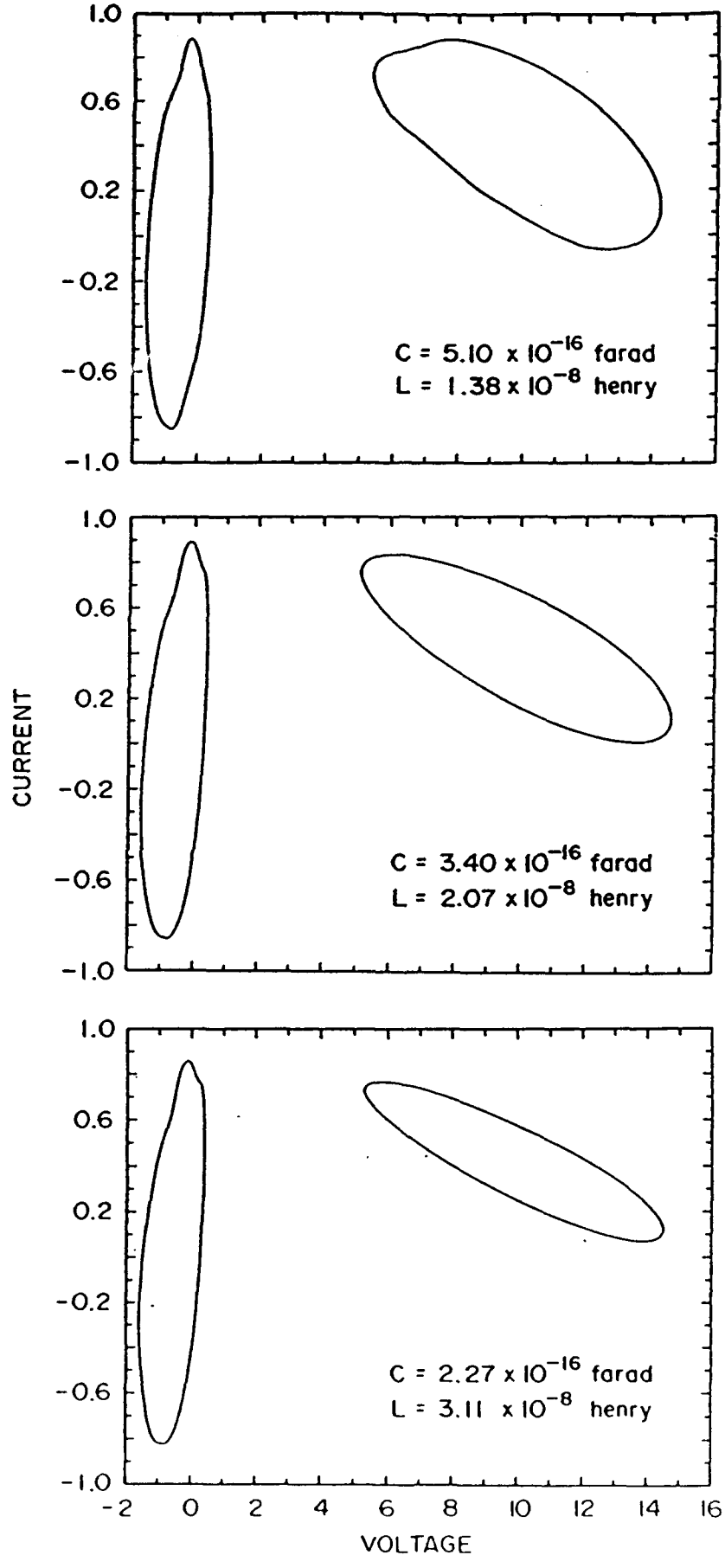

Figure 7. Gate and Drain Current-Voltage Lissajous for $V_g(0) = -0.6$, $V_g = 1.0$, $f_r = 60$ GHz, $f = 40$ GHz and different combinations of inductance and capacitance.

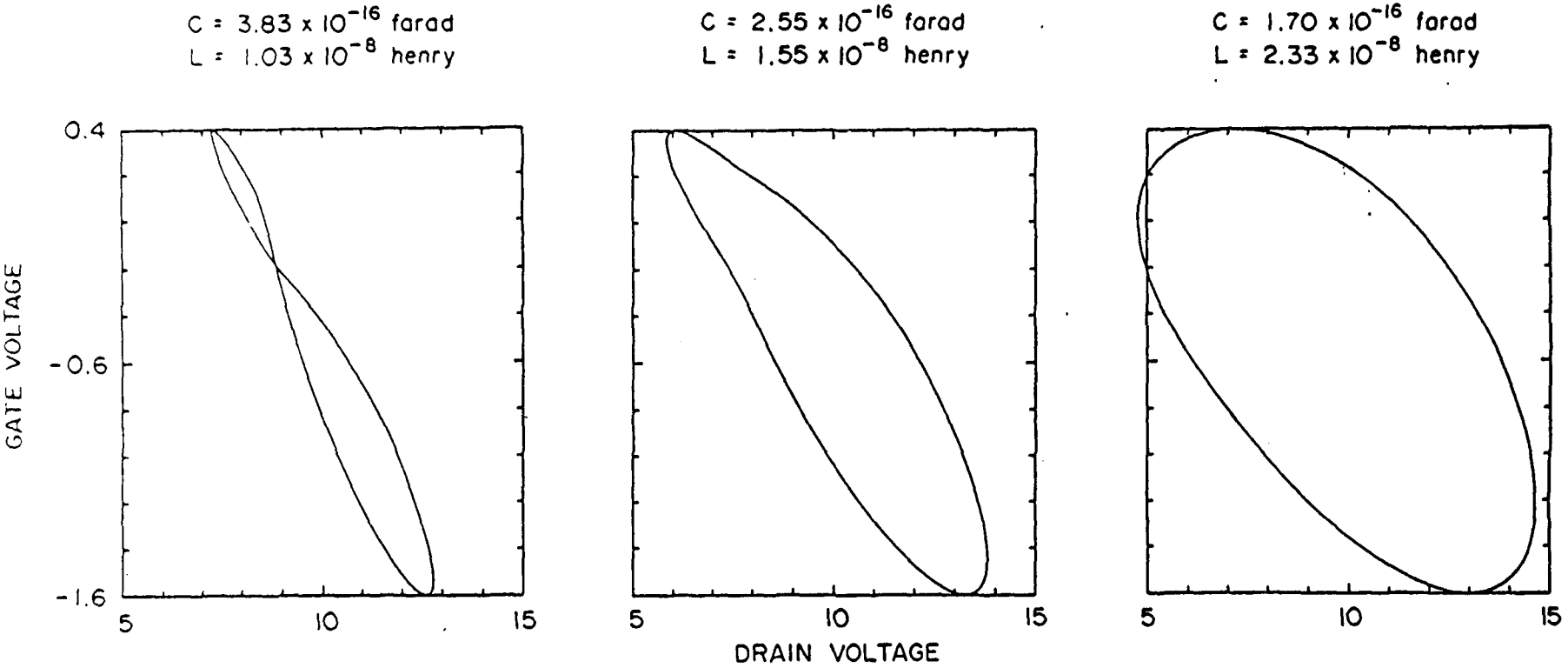

Figure 8. Gate Drain Voltage Lissajous for $V_g(0) = -0.6$, $V_g = 1.0$, $f_r = 80$ GHz, $f = 40$ GHz and different combinations of inductance and capacitance.

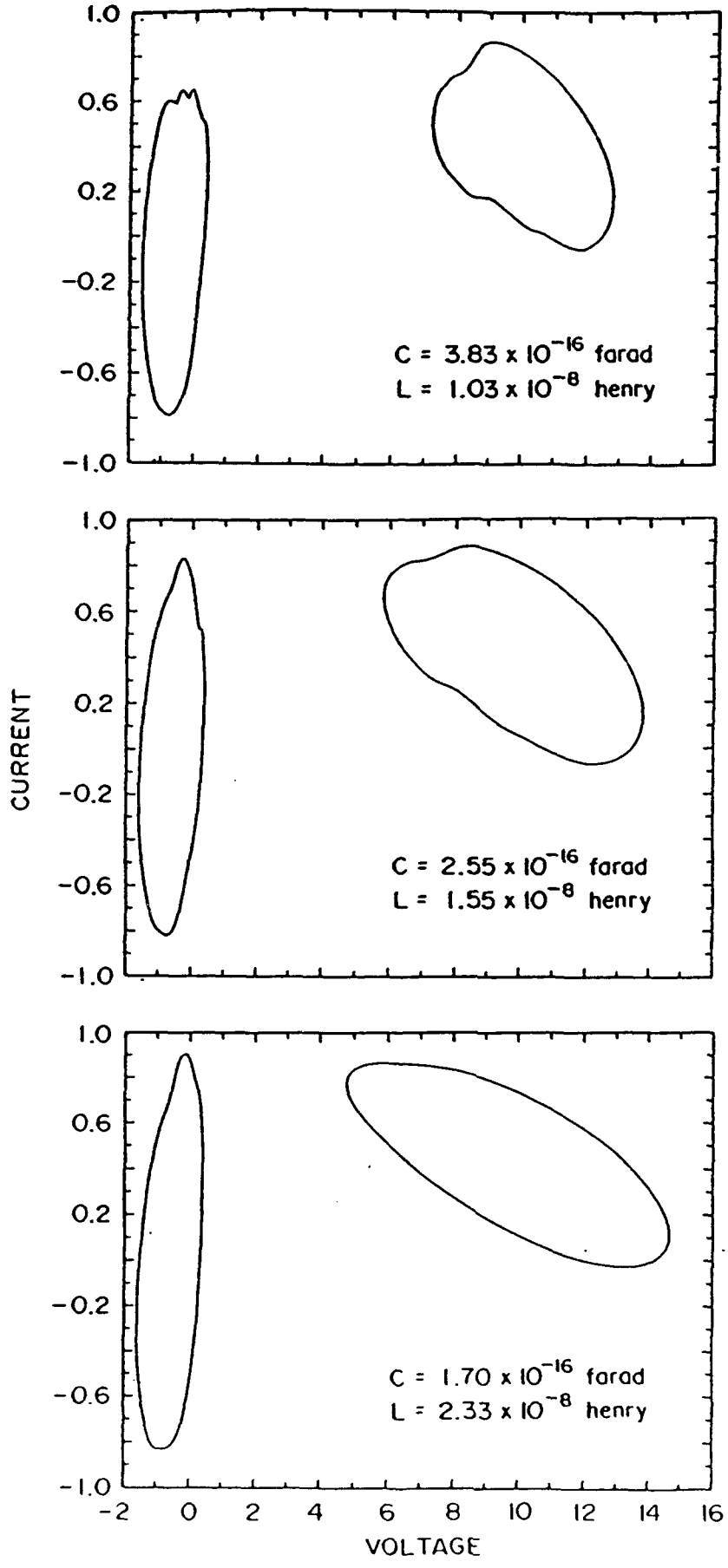

Figure 9. Gate and Drain Current-Voltage Lissajous for $V_q(0) = -0.6$, $V_\varsigma = 1.0$, $f_r = 80$ GHz, $f = 40$ GHz and different combinations of inductance and capacitance.

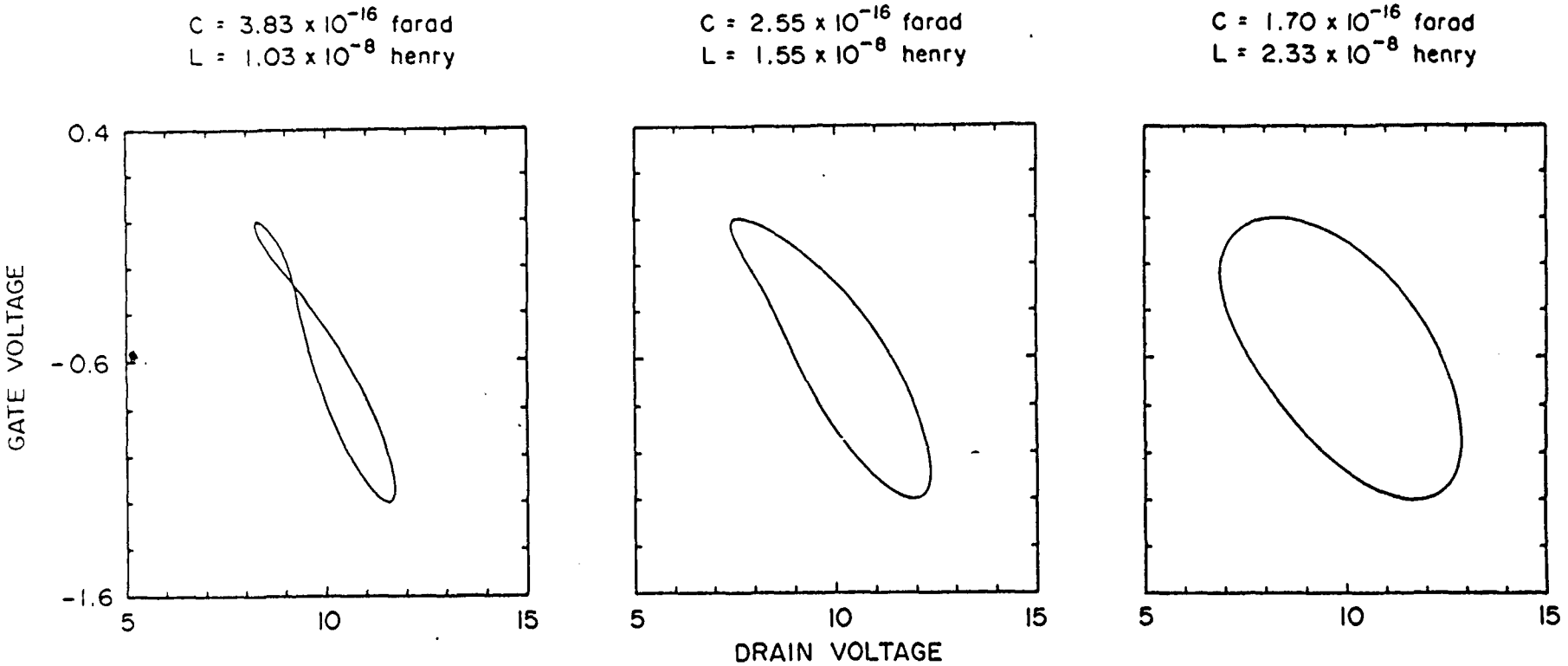

Figure 10. Gate Drain Voltage Lissajous for $V_g(0) = -0.6$, $V_g = 0.6$, $f_r = 80$ GHz, $f = 40$ GHz and different combinations of inductance and capacitance.

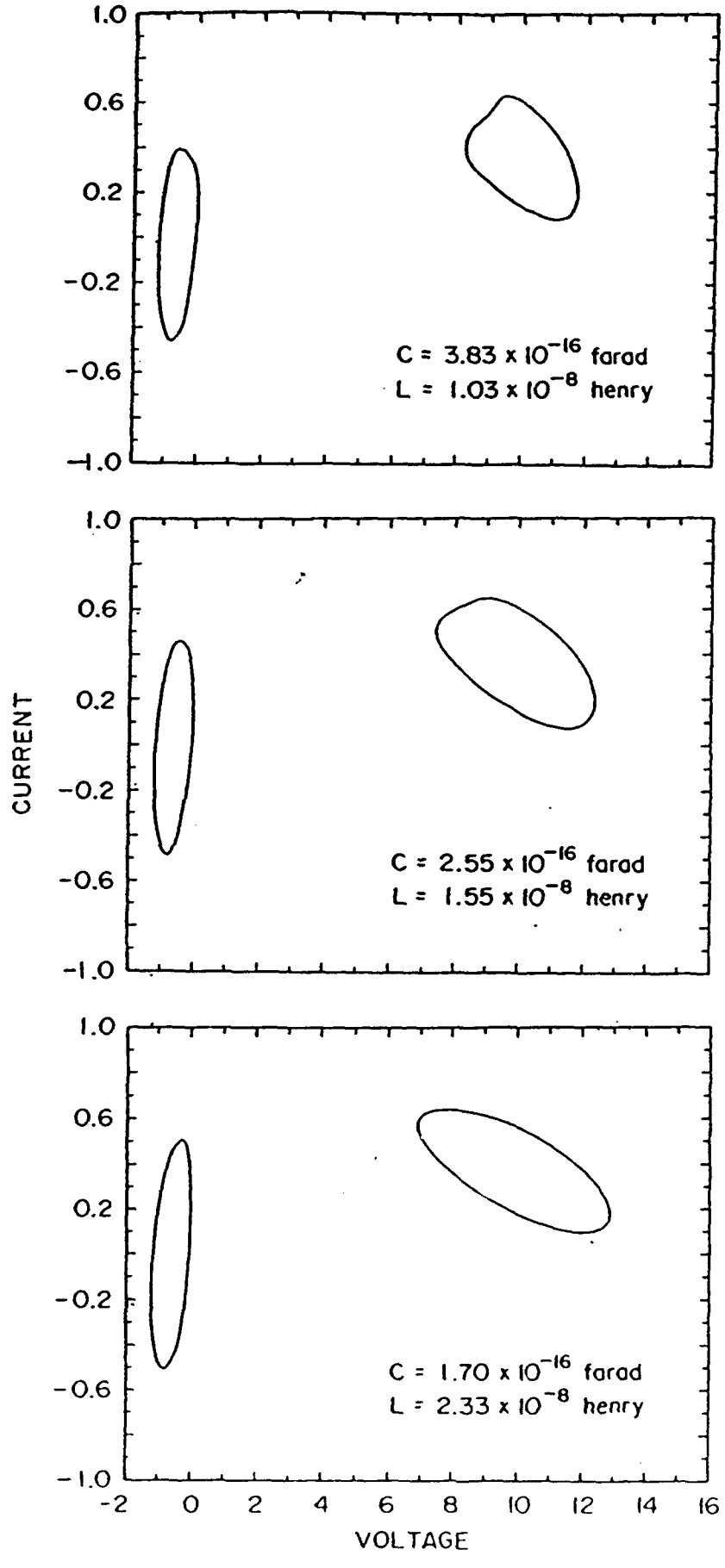

Figure 11. Gate and Drain Current-Voltage Lissajous for $V_g(0) = -0.6$, $V_g = 0.6$, $f_r = 80$ GHz, $f = 40$ GHz and different combinations of inductance and capacitance.

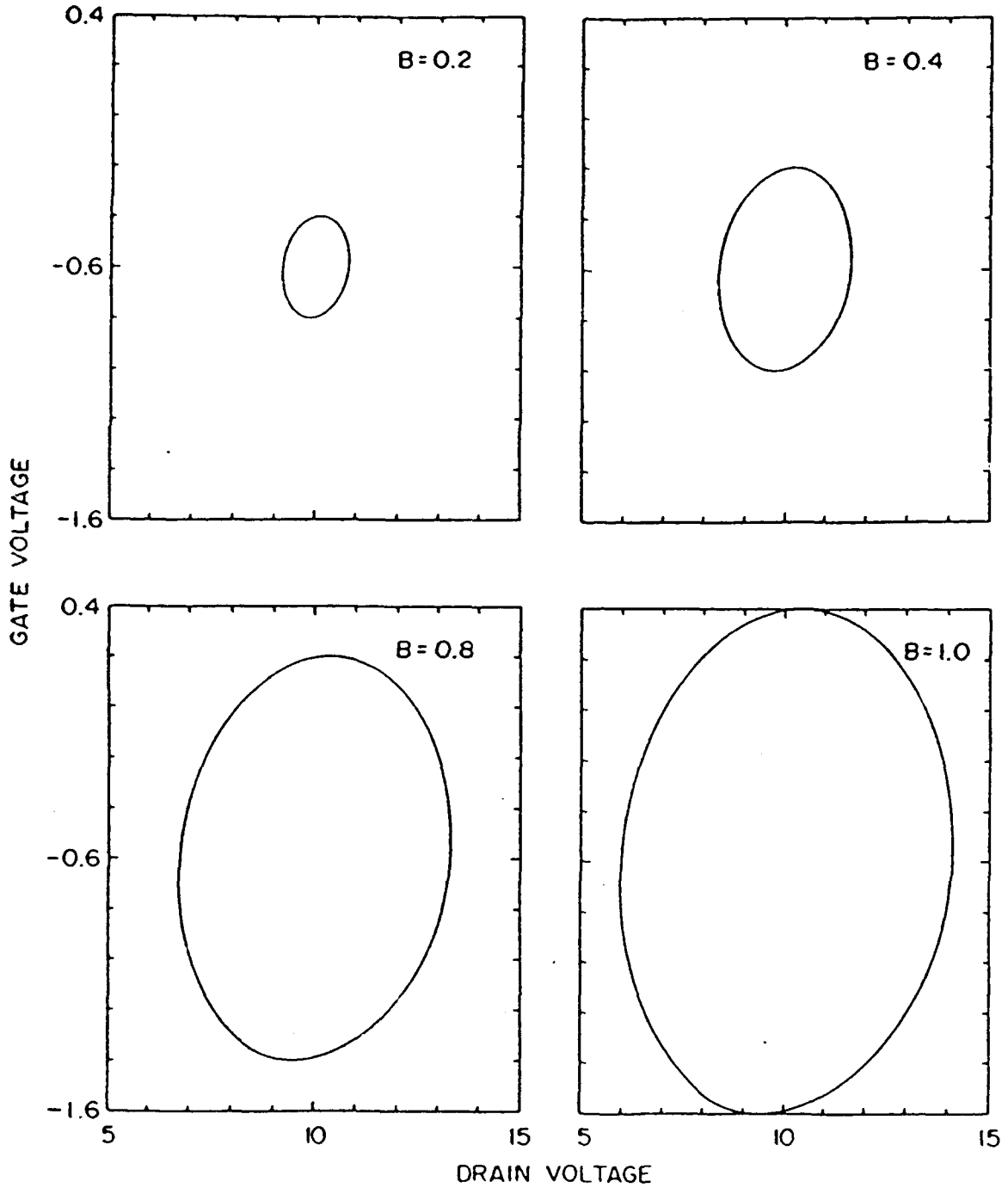

Figure 12. Gate and Drain Lissajous for $V_g(0) = -0.6$, $V_g = B$, $f_r = f = 40$ GHz.

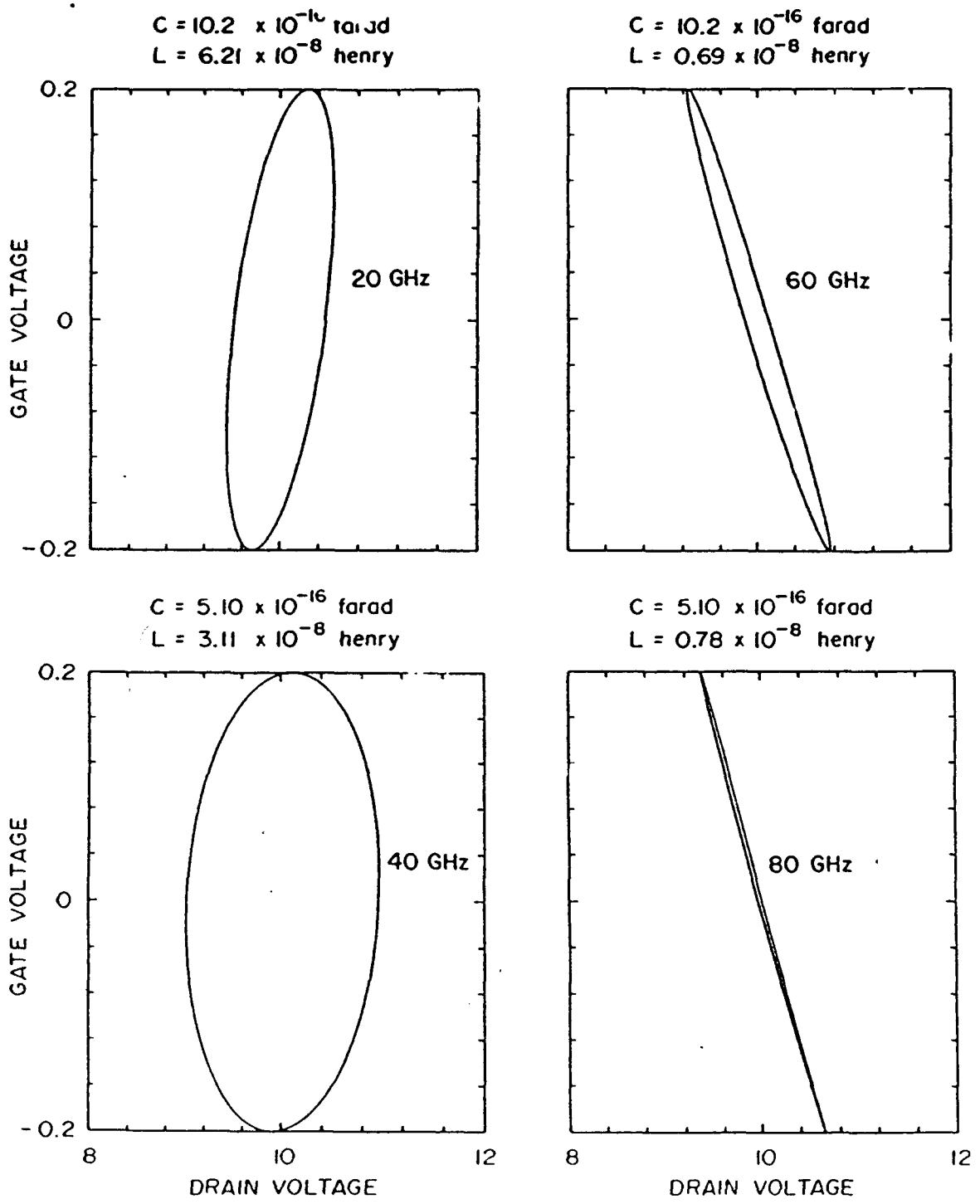

Figure 13. Gate and Drain Lissajous for $V_g(0) = 0.0$, $V_g = 0.2$, $f = 40$ GHz, and f_r as indicated.

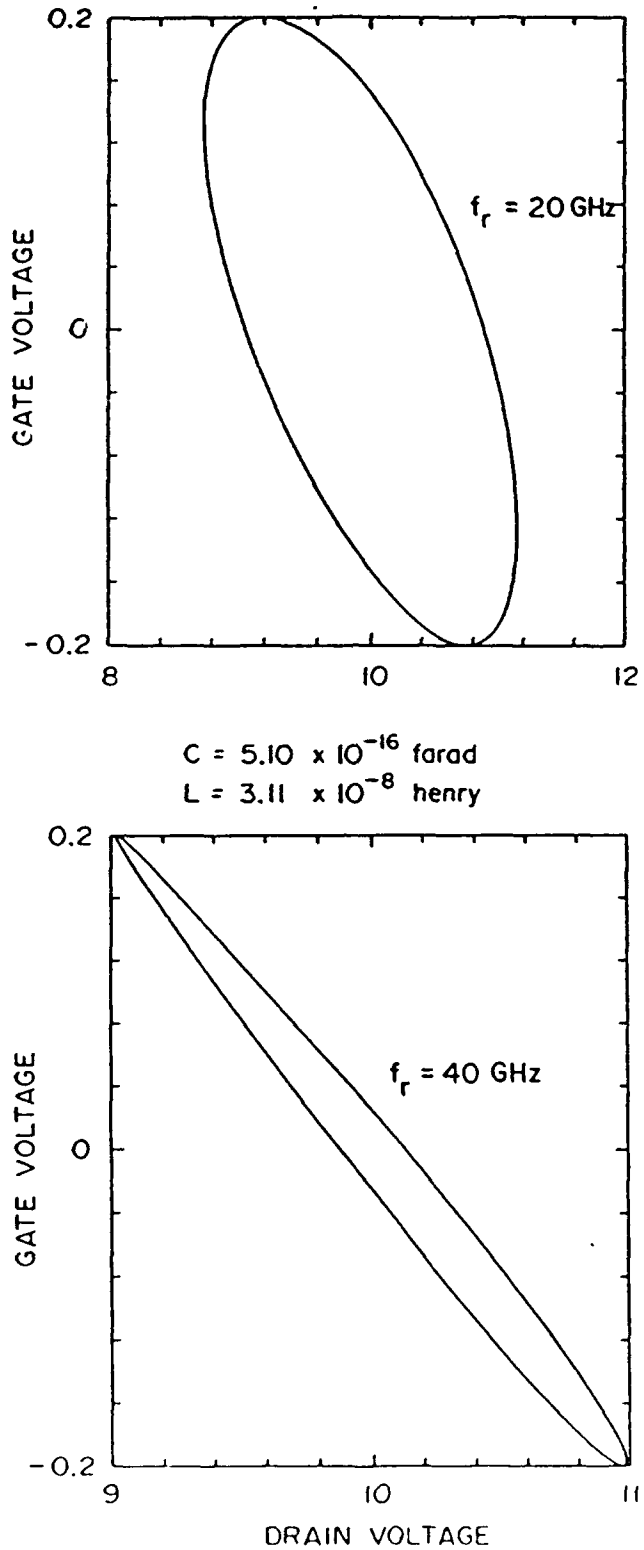

Figure 14. Gate and Drain Lissajous for $V_g(0) = 0.0$, $V_q = 0.2$, $f = 20$ GHz, and f_r as indicated.

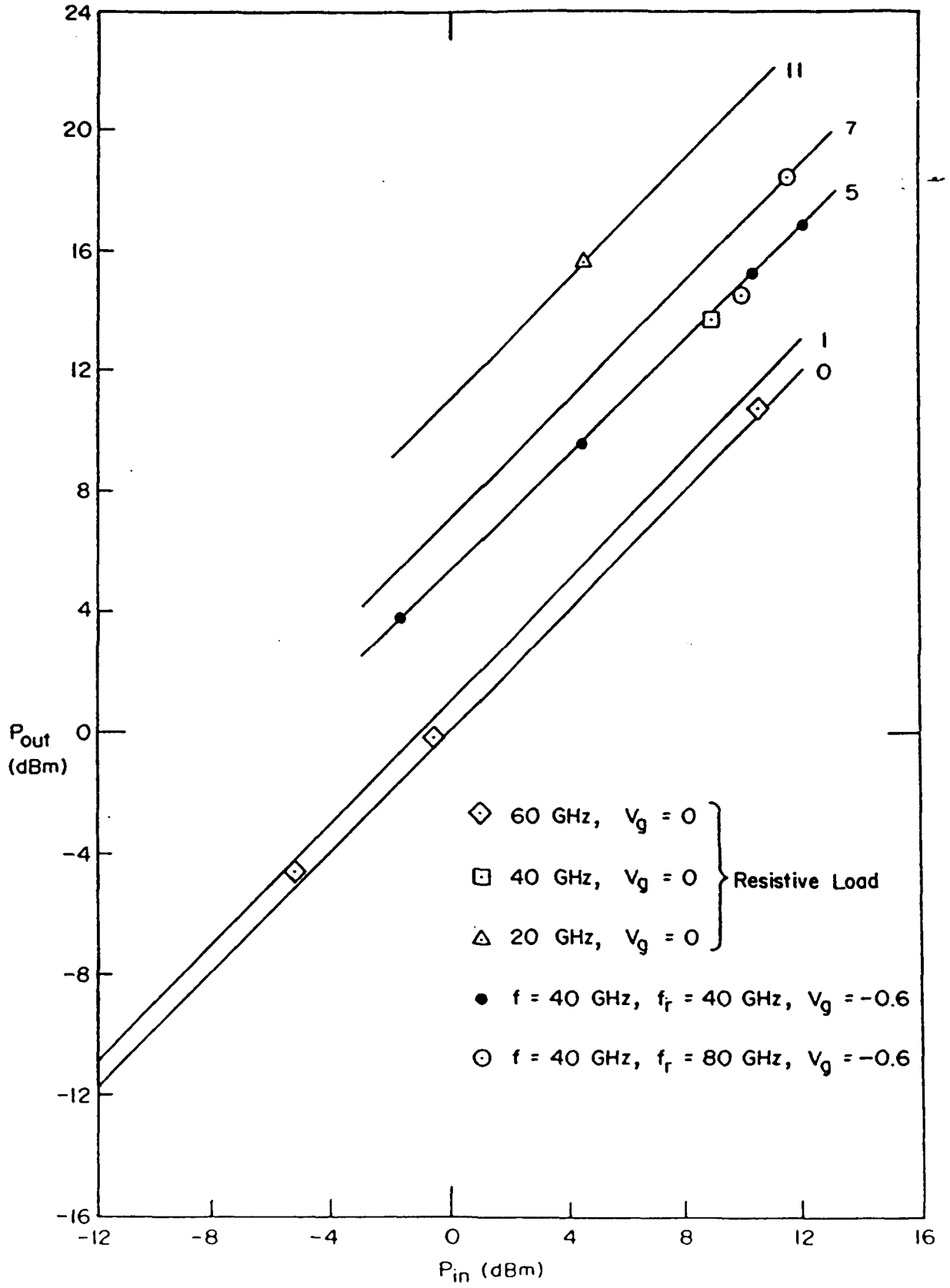

Figure 15. Power gain at select points for 150 identical PBT structures, with 25μm depth. Straight lines are drawn for reference.

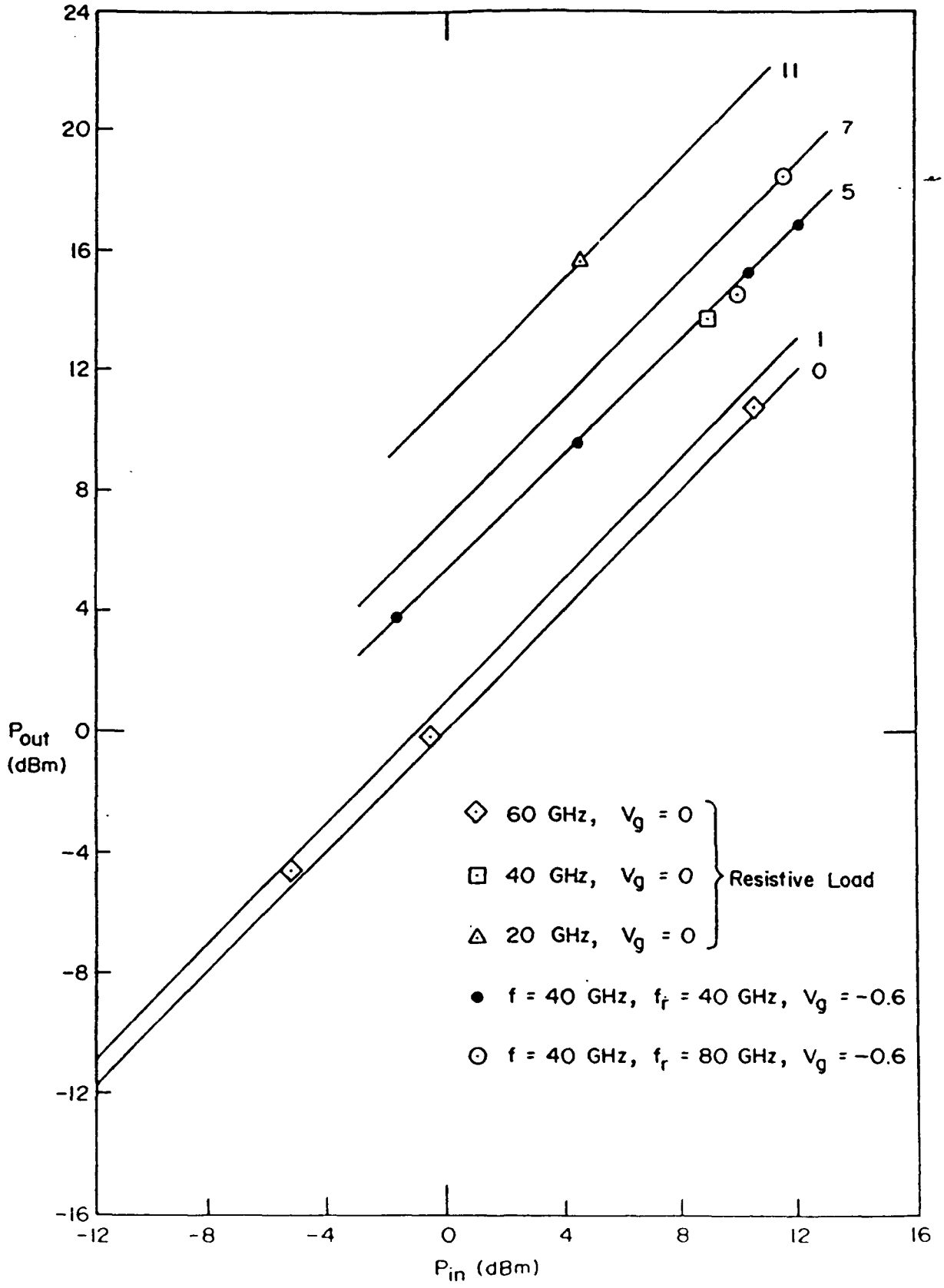

Figure 15. Power gain at select points for 150 identical PBT structures, with 25μm depth. Straight lines are drawn for reference.